Durability of Electrolytes Applied to Printed Field-Effect Transistors

Beständigkeit von Elektrolyten, eingesetzt in gedruckten Feldeffekttransistoren
Zur Erlangung des Grades eines Doktors der Naturwissenschaften (Dr. rer. nat.)
genehmigte Dissertation von Dipl.-Phys. Falk von Seggern aus Summit, NJ (USA)
Tag der Einreichung: 23.03.2017, Tag der Prüfung: 26.04.2017
Darmstadt 2017 — D 17

1. Gutachten: Prof. Dr.-Ing. Horst Hahn
2. Gutachten: Prof. Dr. Jasmin Aghassi

TECHNISCHE
UNIVERSITÄT
DARMSTADT

Fachbereich Material-
und Geowissenschaften

Gemeinschaftslabor Nanomaterialien

Durability of Electrolytes Applied to Printed Field-Effect Transistors
Beständigkeit von Elektrolyten, eingesetzt in gedruckten Feldeffekttransistoren

Genehmigte Dissertation von Dipl.-Phys. Falk von Seggern aus Summit, NJ (USA)

1. Gutachten: Prof. Dr.-Ing. Horst Hahn
2. Gutachten: Prof. Dr. Jasmin Aghassi

Tag der Einreichung: 23.03.2017
Tag der Prüfung: 26.04.2017

Darmstadt 2017 — D 17

Abstract

Field effect transistors (FETs) are indispensable for our modern digital society, needed as basic building blocks for logical gates in all digital circuits. FETs are found in sample and hold circuits with high storage capacities and high write and read speeds and in driver circuits for active matrix displays such as large area TVs. An entire new application perspective is currently emerging in the area of printed electronics, where flexible plastic foils, papers and textiles become inexpensive substrates for novel devices. To realize circuits on such substrates, dielectrics, semiconductors and conductors with suitable morphologies as well as innovative device architectures have to be developed. Prominent among others, printed liquid electrolytes with high gate capacities in combination with printed oxide semiconductors have yielded good device performance and remarkable drain currents at low gate voltages. To be usable in everyday applications basic requirements have to be fulfilled, such as functional stability during environmental temperature changes, sufficient current output to drive more advanced electronic circuits, high switching speed and miniaturized size to allow for large packing densities. Miniaturized high current transistors with good temperature stability can open the path to many new applications for printed electronics, e.g., wearable electronics or lighting solutions, where higher currents are necessary.

In this thesis in-plane indium oxide based FETs have been fabricated utilizing composite solid polymer electrolytes (CSPEs) for gating. Different CSPEs have been investigated to determine the most suitable candidate for high performance FETs concerning chemical, physical and electrical behavior. The CSPE, containing $LiClO_4$, PVA, PC and DMSO, has been selected and printed onto an in-plane electrolyte-gated FET (EG-FET). Special attention has been drawn to the key parameters of the EG-FET like mobility, on-current, on/off-current ratio and threshold voltage tested over a wide temperature range. Especially the temperature independence of the on-current and the threshold voltage as well as the absence of hysteresis turn out to be beneficial with respect to future applicability of printed EG-FETs in electrical circuits.

In order to downsize the in-plane EG-FETs and to obtain large drain currents at the same time, a vertical arrangement of the FET (v-FET) has been realized. In order to achieve this goal, porous SnO_2 has been stacked in between two platinum electrodes to achieve the vertical source/semiconductor/drain structure, in plane with the platinum gate. The gating is realized by inkjet printing a CSPE film covering the semiconductor channel and the gate. The CSPE, infiltrated into the porous semiconductor network, addresses the entire inner surface of the semiconductor. A channel of 45 nm is achieved by utilizing the thickness of the printed semiconductor film. A device using such geometry yields nearly ideal transistor characteristics with a clear current saturation with increasing drain voltage and a quadratic increase of the output curves with increasing gate voltage.

The large drain current densities exceeding 0.1 MA/cm^2 can be explained by the large channel area or channel width, which can be modeled by a large number of independent pillars forming conducting pathways between source to drain electrode.
Finally, the problem of limited switching speeds of an in-plane EG-FET has been addressed. The limiting factor for such devices is clearly the large gate-to-channel distance, which limits the time to form the FET conducting channel. The characteristic time constant is determined by the ionic conductivity of the CSPE and double layer capacitance of the CSPE/semiconductor interface. In order to reduce the gate-to-channel distance, i.e., the total resistance, a back-gated EG-FET has been designed using a porous Al_2O_3 spacer with a thickness of about 300 nm and a porous SnO_2 layer as the channel material. Due to the reduction of the gate-to-channel distance by more than two orders of magnitude a potential reduction of the the switching frequency can be shown.

Abstract

Eine moderne Elektronik ohne Feldeffekttransistoren (FET) ist heute undenkbar. Diese Bauelemente agieren als elektronische Schalter in logischen Gattern und sind im Besonderen in digitalen Schaltkreisen nicht zu ersetzen. Man findet FET sowohl in „sample-and-hold“ Schaltungen für große Datenspeicher mit schnellen Lese- und Schreibzyklen als auch in großflächigen Aktiv-Matrix-Ansteuerungen, wie sie in Displays für Flachbildfernseher benötigt werden. Zur Reduktion der Fertigungskosten solcher Ansteuerungen eröffnet sich derzeit gerade ein neues Wissenschafts- und Anwendungsfeld, dass das Potenzial einer "Druckbaren Elektronik" evaluiert. Dabei werden billige und flexible Substrate wie Plastikfolien, Papier oder Textilien aber auch neue Materialien und Bauteilarchitekturen eingesetzt. Um funktionierende Bauteile herzustellen, benötigt man sowohl leitende, halbleitende als auch isolierende Materialien, die auf solche Substrate gedruckt werden können. Eine Möglichkeit ist dabei, einen leitfähigen flüssigen Elektrolyten als Gate-Dielektrikum in Kombination mit einem gedruckten oxidischen Halbleitermaterial einzusetzen. Solche Materialkombinationen ermöglichen es, sehr hohe "Drain"-Ströme bei niedrigen "Gate"-Spannungen zu erzielen. Für ein Bauteil müssen dazu einige grundlegende Voraussetzungen erfüllt sein, wie z.B. ein stabiler Betrieb bei Temperaturänderung, ein ausreichender "Output"-Strom, um elektronische Schaltkreise betreiben zu können, möglichst hohe Schaltgeschwindigkeiten und eine hohe Packungsdichte, damit solche FET in komplexeren Schaltungen auf kleinem Raum verarbeitet werden können. Bei Gelingen einer solchen Miniaturisierung unter Beibehalt der notwendigen Output-Ströme und eines stabilen Betriebs unter Temperaturänderung eröffnet sich ein neuer Markt für die Druckbare Elektronik, die z.B. Felder wie „Smart Textiles“ oder Beleuchtungsanwendungen umfasst.

In dieser Arbeit wurden planare Feldeffekt-Transistoren mit einem Kanal aus Indiumoxid und einem Komposit-Polymer-Elektrolyt (engl.: composite solid polymer electrolyte (CSPE)) als Gate-Dielektrikum hergestellt. Es wurden verschiedene Komposit-Polymer-Elektrolyte analysiert, um den am besten geeigneten Elektrolyten in Bezug auf chemische, physikalische und elektrische Eigenschaften zu finden. Der letztendlich verwendete Elektrolyt setzte sich aus $LiClO_4$, PVA, Propylencarbonat und Dimethylsulfoxid zusammen und wurde in einem planaren FET als gedrucktes Gate-Dielektrikum eingesetzt. Bei der Funktionsevaluierung wurde besonderes Augenmerk auf die Schlüsselparameter Feldeffektmobilität, on-Strom, on/off-Strom Verhältnis und Schwellspannung gelegt und deren Verhalten in einem weiten, alltagsrelevanten Temperaturbereich untersucht. Insbesondere die Temperaturunabhängigkeit von on-Strom und Schwellspannung und das Fehlen einer Strom-Hysterese in den Transfer-Kurven zeigt das Potential solcher Transistoren für zukünftige Anwendungen in komplexeren elektronischen Schaltungen.

Um die geforderte Miniaturisierung der planaren FET in Kombination mit hohen Output-Strömen zu realisieren, wurde das Konzept eines vertikalen Feldeffekttransistor entwickelt und realisiert. In diesem Zusammenhang wurde ein poröser Halbleiter (SnO_2) zwischen zwei parallelen Platin-Elektroden in einer Sandwich-Geometrie aufgebaut, die als Source- bzw. Drain-Elektrode agieren, was die vertikale Struktur begründet. Die Gate-Elektrode wurde wiederum in planarer Geometrie aufgebaut. Durch das Aufdrucken des CSPE auf die Gate-Elektrode und den Halbleiter und das Eindringen des CSPE in den porösen Halbleiter wird ein Schalten des Bauteils ermöglicht. Durch das Infiltrieren des CSPE in die poröse Halbleiterstruktur wird die gesamte innere Oberfläche des porösen Halbleiters kontaktiert und agiert als Transistorkanal. Auf diese Weise wurde eine Kanallänge des FETs von 45 nm erzielt, was der Schichtdicke des gedruckten Halbleiters entspricht. Die hergestellten Bauteile zeigen nahezu ideale Transistorcharakteristiken, wie z.B. eine vollständige Sättigung des Drain-Stroms bei hohen Drain-Spannungen und einem quadratischen Anstieg des Drain-Stroms mit der Gate-Spannung. Die Stromdichte des Drain-Stroms erreicht dabei Werte von mehr als $10^5\,A/cm^2$ und kann mit der großen Oberfläche des Transistorkanals erklärt werden, die ein Synonym für eine große Kanalbreite ist. Mit einem in dieser Arbeit verwendeten Säulen-Modell war es möglich, die nicht direkt zugängliche experimentelle Kanalbreite zu bestimmen.
In einem letzten Schritt wurde die begrenzte Schaltgeschwindigkeit solcher Elektrolyt-basierter FET mit versetzter Gate-Elektrode evaluiert. Als limitierender Faktor zeigte sich hier eindeutig der große Abstand zwischen Gate-Elektrode und Kanal. Die limitierende Zeitkonstante wird in diesem Fall durch das Produkt des Gesamtwiderstandes des CSPE und der Doppelschichtkapazität der Grenzfläche zwischen CSPE und Halbleiter bestimmt. Um den Abstand zwischen Gate-Elektrode und Kanal und somit auch den Gesamtwiderstand zu reduzieren, wurde ein FET konstruiert, dessen Gate-Elektrode auf der Rückseite des Kanals angeordnet ist. Als Abstandshalter wurde eine 300 nm dicke, poröse Al_2O_3-Schicht verwendet. Diese Bauteile zeigen sehr gute Transistoreigenschaften und der reduzierte Abstandes zwischen Gate-Elektrode und Kanal um den Faktor 100 verspricht eine Verkürzung der Schaltzeit um eben diesen Faktor.

Contents

1 Introduction

First printing dates back to the Mesopotamian civilization before 3000 B.C.. Printing since then is used to print texts, pictures and patterns on various substrates. Earliest reports of woodblock printing or stamping from $\sim$200 A.D. show wide use throughout Eastern Asia [1]. During that time printing was performed mainly on clothes. About 1200 years later the movable type printing was developed, which used separate printing blocks for letters and symbols to make the technique more flexible. Different materials were employed to prepare these blocks, e.g, porcelain, metal and wood. Another 400 years later Gutenberg and Dritzehen invented the printing press, which again increased printing speed and accuracy. The next step towards high throughput printing was done in 1843 when Hoe invented the rotary printing press. In the following years, new techniques for large area printing were developed and optimized like offset, rotogravure, screen and many other techniques.

A big step forward in terms of flexibility and precision was made with the invention of digital printing techniques. In 1867 the first inkjet nozzle was used for recording telegraph signals. The jetting was continuous and the deflection of the nozzle was realized by a magnetic coil. It took another 84 years until the first commercial inkjet printer was presented by Siemens. The next step of development brought the drop on demand (DOD) technique (by Endo and Vaught) in the late 1970s. They found that heating the ink to a sufficient temperature makes a drop eject from the nozzle. Shortly after the introduction of the thermal inkjet the piezoelectric DOD printing was invented, which increased the range of usable inks. The reason for this improvement is that in the latter case, no volatile components are needed and the problem of residue and clogging of the nozzle in the heated region are avoided. Nowadays the piezoelectric DOD is the most common form of modern inkjet technology.

The field of printed electronics has developed around 1990 and is closely linked to the development of functional organic compounds, such as electric conductors, semiconductors and dielectrics. Many different structures, e.g., passive leads, resistors, field-effect transistors (FETs), organic light emitting diodes (OLEDs) and large area devices, such as solar cells are fabricated by printing nowadays. Organic materials are the dominant representatives because of their easy solution processability. Initially, mostly metal electrodes were utilized for contacting and gating but at later stage of development it was possible to fabricate all organic devices. Due to the continuous problems with long term stability of organic devices and compounds, scientists started to direct their interest to printable inorganic oxide semiconductors as active components for FETs. Two types of semiconductors are distinguished, namely hole (p) and electron (n) semiconductors depending on the type of doping. Most of the organic semiconductors show p-conducting behav-

ior, however, their oxide counterparts are commonly n-conducting. The electron conductivity is related to the doping mechanism of the metal oxide semiconductors, where (double) negatively charged oxygen vacancies in the semiconductor establish the predominant doping mechanism. For electronic devices it is important to have both p- and n-type semiconductors. For oxide semiconductors, some candidates for p-type have been reported in literature [2]. In terms of their environmental stability and performance, oxide based semiconductors are inherently superior to their organic counterparts. However, the comparison of synthesis, processing and compatibility with available flexible substrates puts organic materials in the advantage. For organic materials no high temperatures are needed during preparation and thus inexpensive substrates like PEN (polyethylene naphthalate) or PET (polyethylene terephthalate) can be used. Even though there is a competition between the organic and inorganic scientific communities, the combination of both classes of materials in hybrid devices, p-type organic and n-type inorganic materials could offer new opportunities. In this context, CMOS like logic gates could be realized. Such gates are the essential building blocks of all modern electronics and could open new perspectives for printed devices.

Field-effect transistors as mentioned above are the basis for almost all modern electronic devices and act as electronic switches. In such a switch a current through a semiconductor flowing between two terminals, named source and drain, can be controlled by means of an electric field. This electric field is generated by applying a gate voltage to a gate electrode, which is coupled via a gate insulator to the semiconductor. Through the capacitively coupled gate charges are pulled into the semiconductor channel, whose amount is controllable through the amplitude of the applied gate voltage over a wide range. In this way, the amount of charge determines the current between the source and drain electrodes. In general, the accumulation of charge in a semiconductor through an electric field applied across the dielectric is called field-effect. Commonly, the gate insulator materials are solid dielectrics but in the last few years an alternative approach utilizing electrolyte solutions and ionic liquids has been employed. The advantage of electrolytes is their ability to form extremely large capacitances by ion separation in the electric field. Thereby they form atomically or molecularly thin electrical double layers. The formation of electrical double layers is not lost even when the electrolyte or ionic liquid is solidified, e.g., by the addition of a polymer. The rearrangement of the ions within the double layer forced by the gate voltage to a metal conductor or semiconductor creates a very large electric field. This field now is responsible for the field-effect and turns out to be especially beneficial to work effectively as gate dielectric in printed field-effect transistors.

In this thesis two different topics of electrolyte-gated oxide electronics will be discussed: first, the mechanical and thermal stability of printed composite solid polymer electrolytes (CSPEs) in FETs will be investigated and second, a new electrolyte-gated FET (EG-FET) geometry will be introduced, which circumvents the limited printing resolution of commercial printers by using a novel vertical transistor geometry. After introducing the fundamentals related to the present

thesis in Chapter 2 and the experimental framework in Chapter 3, Chapter 4 is the first of two chapters reporting on the experimental results and presents a comprehensive study of the chemical, mechanical and electrical properties of composite solid polymer electrolyte. Based on these CSPEs low voltage printed FETs are prepared and tested with respect to temperature. Therefore key factors of CSPE based FETs have been investigated and their temperature dependence has been recorded in the range of -35 °C to +60 °C and compared with the theoretically expected behavior. The aspect of low voltage/low power consumption is essential to allow for long lasting use in battery powered devices and the aspect of temperature stability of FETs is essential for a stable operation in electronic circuits under normal environmental conditions. The latter point involves not only the heat generated by the transistor itself but also the environmental aspect of being exposed to ambient temperature differences of several tens of degrees in everyday use. In the second chapter of experimental results (Chapter 5) a novel EG-FET geometry will be introduced using the film thickness of a printed film as the channel length instead of the lateral dimension of the semiconductor channel, determined by the spatial resolution of the printer employed. By means of introducing pores in the semiconductor through adding a micelles forming polymer to the semiconductor precursor ink, networks of polymer and semiconductor precursor are formed during drying and annealing. After annealing a porous, crystalline semiconductor has been formed, which can be infiltrated by the CSPE. Using proper contacts it will act as a vertical transistor (v-FET). The obvious advantages are a shorter channel length in combination with higher drive currents. Applying this new design the limited printing resolution of commercial inkjet printers can be circumvent by utilizing the printed film thickness instead of the the lateral dimension. This way, the channel length can be reduced by almost three orders of magnitude to less than 50 nm. Such a new design allows for new applications by opening the possibility of fabricating high current transistors for printed electronics.

2 Fundamentals

2.1 Literature Review

In this chapter the inkjet printing technique utilized in this thesis is presented. In addition, a preview of possible upscaling methods is provided. Printed or partly printed devices, like solar cells, light emitting diodes and field-effect transistors, are described and some challenges in printed electronics are discussed.

2.1.1 Printing Techniques

For the realization of functional devices, several printing techniques have been developed over the last decades. They range from high throughput, large area roll-to-roll compatible printing techniques to sheet by sheet techniques with lesser throughput like digital drop-on-demand (DOD) printing. Roll-to-roll printing techniques are defined by a continuous printing process performed while the substrate (commonly a polymeric foil) is unwound from one cylinder and rewound on another. In the sheet by sheet process substrates are idling during the actual printing process and are exchanged after the printing of each sheet has finished. In industrial and academic use roll-to-roll as well as sheet by sheet based techniques have individual advantages and find their dedicated field of application. Since inkjet printing as a digital drop-on-demand technique is based on a sheet by sheet process, it, in general, serves the requirements of academic problems best, because of the inherent flexibility. In this thesis inkjet printing has been used exclusively and will be presented in more detail in the following paragraphs. A short overview on upscaling possibilities of the printing process using roll-to-roll techniques is presented at the end of this section.

Inkjet printing is a digital printing technique without any need of a physical printmaster. To create the desired structures, the printhead is moved relative to the substrate and ink drops are ejected wherever needed. The layout of the printed structure is created on a computer and can be changed easily. For inkjet printing three mechanisms have been established for the drop formation. These mechanisms are based on different principles which are acoustic, thermal and piezoelectric in nature [3, 4]. The acoustic wave driven method is mostly used for continuous printing applications in industry, e.g., personalization and coding of products as well as packaging. Thereby a piezoelectric crystal creates an acoustic wave, which separates droplets from a continuous flowing stream of ink. In contrast to the continuous acoustic inkjet printing, the thermal and piezoelectric inkjet printing provide drop-on-demand techniques and are used for patterning of more complex

structures. Thermal DOD techniques use a heater in the nozzle region, which heats up the ink to its boiling point and the pressure created by the expansion of the evaporating solvent causes the ejection of a droplet. In the case of piezoelectric supported DOD techniques a piezoelectric crystal is driven by an oscillating voltage, which compresses and releases the nozzle in a sinusoidal manner. For the ejection of a droplet, a pulse signal is overlaid in a way that enough pressure is created to force a droplet to leave the nozzle. The most common and mature technique is the piezoelectric DOD, which has been used exclusively for the experiments throughout this thesis. Inkjet printers for laboratory applications thereby have many possibilities to adjust printing parameters and allow for customizing the printing process to most of the utilized inks and substrates. The technique is capable of printing a large variety of different functional materials, like organic conductors, semiconductors and dielectrics [5–13] as well as inorganic materials like metals for electrodes and leads [14–16] and metal oxides for semiconducting channels or dielectrics. Thereby inorganic functional materials can be prepared in two different ways. One possibility is to use metal-organic compounds or dissolved salts in a suitable solvent as a precursor solution. The second possibility is to disperse stabilized nanoparticles in a solvent [2, 17–23]. The spatial resolution lies at best in the range of 5 μm [6]. The nature of the substrates is variable and can be rigid like glass or silicon wafers as well as flexible like plastic foil or paper, but preferentially has to be flat. A disadvantage is that high throughput is not easily achievable but for laboratory scale applications the advantages are paramount.

For industrial upscaling, different printing techniques can be applied that are compatible with the before mentioned roll-to-roll technique. The most suitable printing techniques are analogue techniques like offset printing [24, 25], flexography [26, 27] and microcontact printing [28]. These printing techniques all utilize physical printmasters and transfer the layout of the printmaster to the substrate by direct contact printing. The masters are made of different materials like metal and rubber, and are prepared by various lithographic processes. The achievable resolution ranges from 1 to 100 μm depending on the individual printing technique and the available ink. Especially, electrodes and leads have been structured using analogue roll-to-roll techniques, which proves that these techniques are capable of upscaling, in general.

2.1.2 Printed Devices

For more than two decades printing has been applied to functional inks with the goal to fabricate active and passive components in electronic devices. Different materials, i.e., metals for leads or electrodes are applied for passive components and organic and inorganic materials as semiconductors and electrolytes for active components. For large area applications such as organic light emitting diodes and solar cells, techniques like dye slot coating are adopted. For more delicate structures like electrodes and active components, digital printing techniques, i.e., inkjet printing

are utilized. Here few of such printable electronic devices and their basic functional principles are described.

- Solar cells utilize semiconductors with a band gap in the energy range of the sunlight to create electron/hole pairs. Those electron/hole pairs are separated by an electric field and the produced electrons and holes are transported to the opposite electrodes of the solar cell. Thereby an electric current is created, which can be utilized to power an external device. A classical solar cell is prepared from crystalline silicon and has the basic structure of a large area photodiode (see Figure 2.1). Such a cell needs highly sophisticated preparation techniques and can presently not be printed entirely. Nevertheless, the top electrodes of such solar cells are frequently printed using metal inks and screen printing techniques. Further, more sophisticated deposition techniques are being explored nowadays [29, 30].

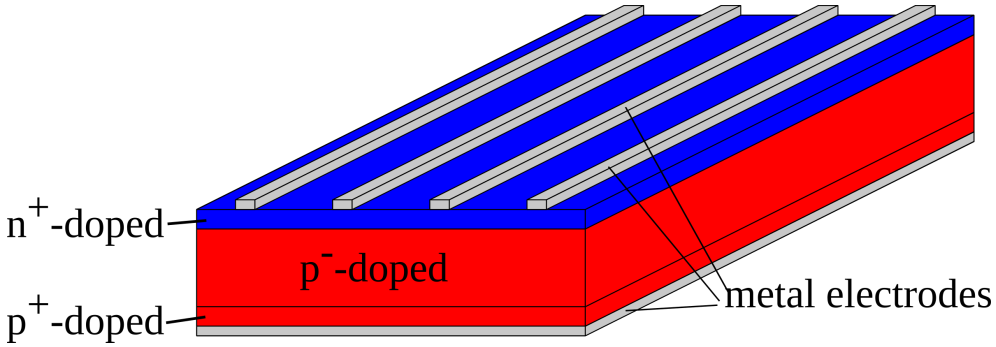


Figure 2.1.: Schematics of a crystalline silicon solar cell consisting of a areal metal back electrode, differently doped regions of a crystalline silicon wafer and thin stripes of metal top electrodes.

A different type of solar cells, in which printing techniques are used more extensively in the production, are thin film solar cells. Several components of such devices are printed nowadays. These cells owe their development to the fact that the absorption of photons in semiconductors basically happens within the first 10 μm. Due to this short penetration depth, thinner absorbing structures can be used, which are easier to be printed. As an additional benefit, the shorter pathways for the electrons and holes to the electrodes allow for a more efficient charge separation and charge collection. Organic polymers and small molecules with semiconducting properties, i.e., mixtures of P3HT[1], PCBM[2], PCPDT-BT[3] and PCDTBT[4] [31–35] are printed as ultra thin functional layers of a few 100 nm with excellent absorption and charge separation properties. The charge separation occurs by a so called bulk heterojunction, which consists of a nanoscale blend of donor and acceptor materials. These donor and acceptor materials allow either electrons or holes to be transported to opposite electrodes and thus generate the photovoltaic current. The voltage results from the

[1] poly(3-hexylthiophene)
[2] (1-(3-methoxycarbonyl) propyl-1-phenyl[6,6]C 61)
[3] poly[2,6-(4,4-bis-(2-ethylhexyl)-4H-cyclopenta[2,1-b;3,4-b']dithiophene)-alt-4,7-(2,1,3-benzothiadiazole)]
[4] poly [N-9"-hepta-decanyl-2,7-carbazole-alt-5,5-(4',7'-di-2-thienyl-2',1',3'-benzothiadiazole)]

different work functions of the two electrodes. To allow the light to penetrate into the solar cell the electrodes are mostly a combination of a metal back electrode and a transparent conductive oxide front electrode. Printing of all organic solar cells are presently hampered by the intrinsically low conductivity of the organic electrodes, which usually limits their efficiency strongly. To improve efficiency, tandem cell structures have been developed to increase the absorption efficiency for the incoming light [36]. For this class of solar cells inkjet printed transparent electrodes made from tin doped indium oxide (ITO) [37, 38] as well as aerosol jet printed active layers [39] have been applied successfully.

Another type of solar cell is the so called Grätzel or dye sensitized solar cell, which shows promising results when printed. Many components of such a dye sensitized solar cell have already been printed successfully: Cherrington et al. used inkjet printed TiO_2 nanoparticles to create the porous network needed for electron conduction [40], Hashmi et al. used the same technique for application of dyes and electrolytes [41, 42] and Dodoo-Arhin et al. prepared graphene inks to fabricate high quality counter electrodes [43]. These devices showed conversion efficiencies in the range of 3 to 7 % with impressive durability.

- Another application of printing techniques is for the fabrication of light emitting diodes (LED). The device structure is similar to a diode but instead of using silicon, germanium or selenium, which are indirect band gap semiconductors, direct band gap semiconductors like GaN, GaAs, etc. are used due to their higher luminous efficiency. Conventional, inorganic LEDs are made from crystalline bulk materials and the contacts are realized by metals to be contacted by subsequent soldering and bonding. The device works as a light source if current is passed through in forward direction whereby electrons are driven from the n-type into the p-type semiconductor region where recombination with holes from the valence band occurs, resulting in the emission of photons with a discrete wavelength according to the band gap energy. If phonons or excitons are involved in the recombination process, the wavelength can be shifted towards lower energies and the emission spectrum broadens.

  In recent years organic LEDs have gained more and more attention and found applications in smartphones, tablets and even TVs. The differences compared to conventional LEDs are the active materials utilized and the preparation methods. The setup is not as simple as for the inorganic LEDs and mostly consists of stacked thin films of different active and passive materials. The simplest design consists of a transparent top electrode (mostly ITO), a hole conductor, a dye consisting layer (active, light emitting layer), an electron conductor and a back electrode with a low work function. For applications several blocking layers have to be included to concentrate the electrons and holes to the emissive layer for higher luminance efficiency. Furthermore, triplet emitter have been included into the emissive layer to allow for efficiencies beyond 25 % circumventing the singlet to triplet ratio. Thin films of different

materials are still deposited by physical vapor deposition and chemical vapor deposition, however, also printing techniques have been applied very successfully in recent times [44–49].

- Another very prominent research and development area is the fabrication of printed field-effect transistors (FETs) intended to serve in inexpensive circuits, e.g., radio frequency identification tags [28]. Their function and physical principles are explained in detail in section 2.2 and are one of the main topics of this thesis. Crucial points are the choice of materials used for the transistor preparation and the utilized geometry. Several materials make up the FET: the semiconductor is responsible for forming the FET channel, the conducting materials are used for electrodes and leads and the dielectrics are used as gate insulators. The channel materials discussed in the literature so far can be divided into three distinct groups: graphene-based semiconductors, organic semiconductors and inorganic semiconductors. For the graphene-based materials, which are applicable in FETs, semiconducting carbon nanotubes [50, 51] and graphene sheets [52] are the most studied modifications. While graphene has many advantages, such as flexibility and temperature stability, a problem arises from the rather low on/off-current ratio [53, 54]. Carbon nanotubes in contrast show high mobility and ambipolar transistor behavior [50, 51], but the production of purely semiconducting carbon nanotubes is still demanding. Organic semiconductors have been studied for the longest time and have improved over the years to overcome many challenges. As an example, degradation under ambient conditions has been an issue for a long time but nowadays show stable performance without any encapsulation over weeks or even months [55]. For high performance devices field-effect mobilities in the range of $> 1\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ are needed, and consequently the field-effect mobility has always been an issue for organic semiconductors as well. Today values of more than $10\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ have been realized under certain idealized preparation conditions [56, 57] for p-type semiconductors, but the lack of equally performing n-type materials is still a major drawback. Recent progress in preparing n-type semiconductors, however, promises a solution to this problem when using small molecule polymer blends. Transistors utilizing n-type semiconductors with mobilities in the range of $0.5\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ have been introduced recently [58]. However, further improvements by one order of magnitude larger electron mobilities are desirable and necessary. Much higher field-effect mobilities for n-type semiconductors are provided by inorganic semiconductors. Some candidates like In_2O_3 show values up to $126\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ even for printed films [20]. Furthermore, the stability in ambient conditions is superior to all organic counterparts [59]. However, the inorganic semiconductors still suffer from various problems, e.g., the need of high temperatures during preparation from precursors to initiate the conversion to metal oxides. When dispersed in the form of nanoparticles, surfactants are necessary to keep the nanoparticles from agglomerating in the ink. These surfactants reduce the performance of the FET drastically. The problem of preparation temperature has been tackled lately and

techniques like UV light to trigger the conversion of precursors or chemical curing to remove the surfactants from the nanoparticles during drying have been successfully employed [19, 60].

2.2 Field-effect Transistors

Field-effect transistors are the most basic components for every modern electronic devices and every logic circuits. Their operating principle is described in detail due to their relevance for this thesis. The generic geometry of an FET is displayed in Figure 2.2. The operating principle is the control of a current between two electrodes, i.e., source and drain, by a voltage applied to a third electrode, the gate. The entire device acts thereby as a current switch. The channel is the region of the semiconductor in between source and drain electrodes, whose electrical properties are changed by the so called field-effect. The field-effect refers to the change of the electrical conductivity of the semiconductor by the application of an external electric field or equivalently by a voltage applied between the semiconductor and gate electrode in Figure 2.2.

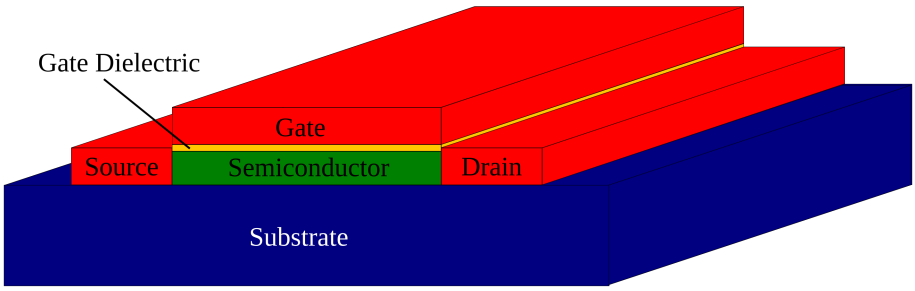


Figure 2.2.: Schematic of a metal oxide semiconductor field-effect transistor showing electrodes (source, drain and gate electrode) in red, gate dielectric in yellow, semiconductor in green and substrate in blue

In the following sections the theoretical background of the field-effect, the transfer characteristics and the output characteristics is presented. Afterwards different transistor geometries are introduced and their influence on the transistor functionality is discussed briefly.

2.2.1 Theory

A metal oxide semiconductor field-effect transistor (MOSFET) is shown in Figure 2.2. The electrical behavior can be best explained on the basis of a capacitor (see Figure 2.3(a)). In the capacitor, two conducting plates (one metal plate and another metalized semiconductor) are separated by a dielectric insulator with a relative dielectric permittivity ϵ_r, a thickness d and an area A. When a voltage V'_{gs} is applied between the two electrodes a charge Q is accumulated according to the

equation $Q = C'_{\mathrm{diel}} \cdot V'_{\mathrm{gs}}$, where C'_{diel} is the capacitance of the device, which can be described by $C'_{\mathrm{diel}} = \epsilon_0\,\epsilon_r\,\frac{A}{d}$ with ϵ_0 the permittivity of vacuum. With the voltage V'_{gs} applied between the back contact (usually a metal) of the semiconductor and the metal electrode (gate), an electric field develops in the dielectric which causes charges to be accumulated in the semiconductor at the semiconductor/dielectric interface counterbalanced by charges of opposite polarity in the metal gate electrode. The injection of charges into the semiconductor, however, requires an ohmic like contact between the semiconductor and metal back contact. At the semiconductor/dielectric interface these charges are distributed over a small thickness within the semiconductor.

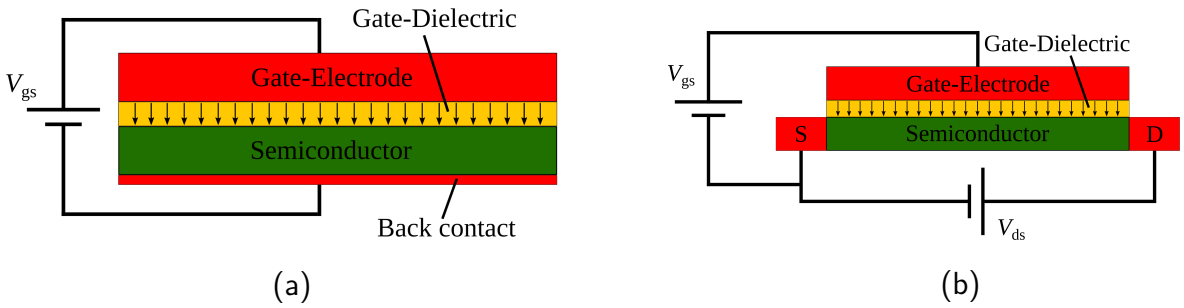


Figure 2.3.: Schematic of the operating principle of (a) a capacitor and (b) a field-effect transistor.

The transistor is then formed by breaking up the back contact of the semiconductor into two contacts placed at the two sides of the semiconductor. These are the source S and drain D of the transistor as shown in Figure 2.3(b). The principle of operation stays basically the same except that an additional voltage V_{ds} is applied across source and drain. For an n-type semiconductor as utilized throughout this thesis, the reaction to a positive voltage V'_{gs}, applied to the gate is the injection of electrons into the semiconductor from source and drain dependent on the relative magnitude of V'_{gs} and V_{gd} (the relative voltage between gate and drain). The current I_{d}, flowing through the semiconductor from source to drain, describes the motion of these electrons driven by the drain voltage V_{ds} and controlled by V'_{gs}. I_{d} can be calculated using the equivalent circuit shown in Figure 2.4. The derivation of the drain current I_{d} has been shown in literature before [61, 62] and will be presented in short form. As a first step the total resistance R_{tot} is calculated as a series of differential resistors $dR(x)$, which results in: $R_{\mathrm{tot}} = \int_0^L dR(x)$, with L the channel length of the transistor. In Figure 2.4 a discrete model is presented where always a resistor $dR(x)$ is coupled to an areal capacitance C_{diel}. Following Ohm's Law the drain current results in $I_{\mathrm{d}} = \frac{V_{\mathrm{ds}}}{R_{\mathrm{tot}}}$. The differential resistance can then be written as [62]

$$dR(x) = \frac{dx}{e\,W\,(\mu_{\mathrm{n}}\,n^*(x)\;+\;\mu_{\mathrm{p}}\,p^*(x))} \tag{2.1}$$

with $\mu_{\mathrm{n,p}}$ the mobility of electrons and holes in the semiconductor and $n^*(x), p^*(x)$ the areal carrier density of electrons and holes, respectively. Since in the case of solely n-type semiconductors, as exclusively used in this thesis, $n^*(x) \gg p^*(x)$ the holes do not have to be considered any further.

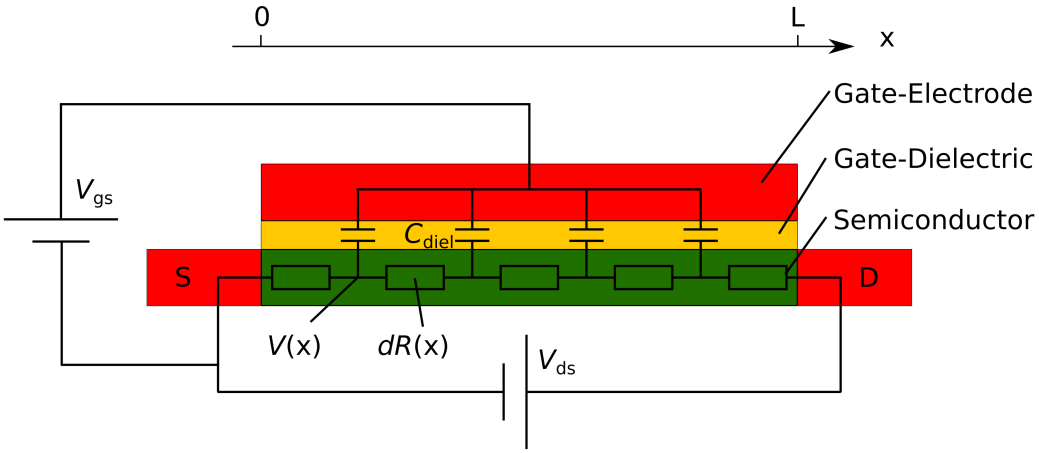


Figure 2.4.: Electrical equivalent circuit of a field-effect transistor based on the description of a transmission line including resistors and capacitors to describe the charge transport and charge accumulation in the device.

The areal charge density $Q^*(x)$ in the channel of the semiconductor can be obtained from the local voltage drop $(V(x) - V'_{\mathrm{gs}})$ over the dielectric by

$$Q^*(x) = -e\, n^*(x) \;=\; C_{\mathrm{diel}}\,(V(x) \;-\; V'_{\mathrm{gs}}) \tag{2.2}$$

where C_{diel} resembles the areal capacitance of the gate/dielectric/semiconductor capacitor. The voltage $V(x)$ for a constant current I_{d} over the entire channel length can be obtained by simple proportionality of a voltage divider

$$V(x) = V_{\mathrm{ds}}\,\frac{R(x)}{R_{\mathrm{tot}}} \quad \text{with} \quad R(x) = \int_0^x \frac{dx}{e\,W\,\mu_{\mathrm{n}}\,n^*(x)} \quad \text{and} \quad R_{\mathrm{tot}} = R(L). \tag{2.3}$$

To derive the differential areal charge density $dQ^*(x)$, eq. (2.2) is differentiated and eq. (2.1) and eq. (2.3) are inserted into the derivative of eq. (2.2). It yields:

$$dQ^*(x) = \frac{C_{\mathrm{diel}}\,V_{\mathrm{ds}}}{R_{\mathrm{tot}}}\,\frac{dx}{e\,W\,\mu_{\mathrm{n}}\,n^*(x)} \tag{2.4}$$

Assuming the voltage $V(x)$ in the channel is steady and monotonous and with the boundary condition $Q^*(0) = C_{\text{diel}}\, V'_{\text{gs}}$ as well as $Q^* = e\, n^*(x)$ the differential equation

$$Q^*(x)\, dQ^* = -\frac{C_{\text{diel}}}{\mu_{\text{n}}\, W}\, \frac{V_{\text{ds}}}{R_{\text{tot}}}\, dx \tag{2.5}$$

can be solved and results in

$$Q^*(x) = -\sqrt{C_{\text{diel}}^2\, V_{\text{gs}}'^2 \; - \frac{2\, C_{\text{diel}}}{\mu_{\text{n}}\, W}\, \frac{V_{\text{ds}}}{R_{\text{tot}}}\, x}. \tag{2.6}$$

The absolute resistance R_{tot} for $V_{\text{ds}} < V'_{\text{gs}}$ can be found with the boundary condition $Q^*(L) = C_{\text{diel}}(V_{\text{ds}} - V'_{\text{gs}})$.

$$R_{\text{tot}} = \frac{2\, L}{\mu_{\text{n}}\, C_{\text{diel}}\, W\, (V_{\text{ds}} \; - \; 2V'_{\text{gs}})}. \tag{2.7}$$

For $V_{\text{ds}} > V'_{\text{gs}}$ the charge density at $x = L$ yields $Q^*(L) = 0$ and from eq. (2.6) the total resistance condenses to

$$R_{\text{tot}} = \frac{2L\, V_{\text{ds}}}{\mu_{\text{n}}\, C_{\text{diel}}\, W\, V_{\text{gs}}'^2}. \tag{2.8}$$

The drain current I_{d} then can be written as $I_{\text{d}} = \frac{V'_{\text{gs}}}{R_{\text{tot}}}$. With the additional introduction of the threshold voltage V_{th} with $V'_{\text{gs}} = V_{\text{gs}} - V_{\text{th}}$, I_{d} shifts to higher values of V_{gs}, and the drain current finally results in

$$I_{\text{d}} = \frac{W}{L}\, C^*\, \mu_{\text{n}}\, (V_{\text{gs}} - V_{\text{th}} - \frac{V_{\text{ds}}}{2})\, V_{\text{ds}} \qquad \text{for } V_{\text{ds}} \le V_{\text{gs}} - V_{\text{th}} \text{ (linear regime) and} \tag{2.9}$$

$$I_{\text{d}} = \frac{W}{2\, L}\, C^*\, \mu_{\text{n}}\, (V_{\text{gs}} - V_{\text{th}})^2 \qquad \text{for } V_{\text{ds}} > V_{\text{gs}} - V_{\text{th}} \text{ (saturation regime).} \tag{2.10}$$

Thereby the threshold voltage V_{th} is related to the areal trap density in the channel by $n_{\text{trap}} = C_{\text{diel}} V_{\text{th}}/d$. With this set of equations the output characteristic curves of a field-effect transistor can be described.

For the analysis two types of measurements are performed: (1) a sweep of V_{gs} with constant V_{ds} and (2) a sweep of V_{ds} with constant V_{gs}. The first one is called transfer characteristics, the latter is called output characteristics. Figure 2.5(a) shows a theoretical transfer characteristic and Figure 2.5(b) theoretical output characteristics of an FET. These two figures describe the dependency of the drain current I_{d} on the drain voltage and gate voltage, respectively. The specific carrier mobility μ_{n} of the material is thereby usually replaced by the device specific

field-effect mobility μ_{FET}. For electrolyte gated FTs as used exclusively throughout this thesis the areal capacitance C_{diel} of the gate/dielectric/semiconductor capacitor is replaced by the areal double layer capacitance C_{dl}.

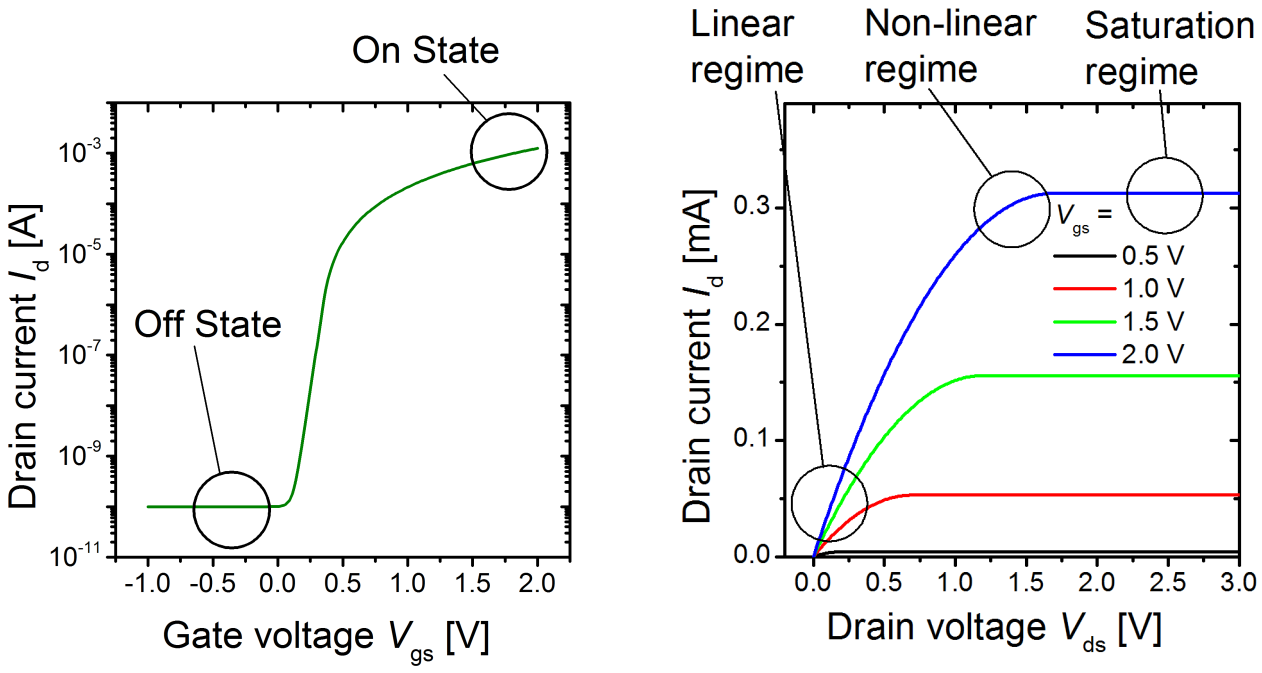


Figure 2.5.: Theoretical transfer curve with indicated off and on state (a) and output characteristic curves with indicated linear, non-linear and saturation regime (b) calculated from eq. (2.9) and (2.10)

Concerning the time constants of an FET, the transit time τ_{transit} describes the time it takes for electrons to drift from source to drain. This time is related to the channel length, the electron mobility of the semiconductor μ_{n} and the applied drain voltage V_{ds} and described by

$$\tau_{\mathrm{transit}} = \frac{L^2}{\mu_{\mathrm{n}} V_{\mathrm{ds}}}. \tag{2.11}$$

The transit time τ_{transit} describes the minimum time an electron needs to travel in the channel from source to drain and thus determines a theoretical cut-off frequency f_{co} of the device:

$$f_{\mathrm{co}} = \frac{\mu_{\mathrm{n}} V_{\mathrm{ds}}}{L^2}. \tag{2.12}$$

2.2.2 Geometry

The geometry of MOSFETs can be designed in many different ways. Two possibilities can be seen in Figure 2.2 and 2.6. On non-conductive substrates mostly a top gate geometry is used, where the gate dielectric is deposited on top of the channel material, followed by the gate electrode (see Figure 2.2).

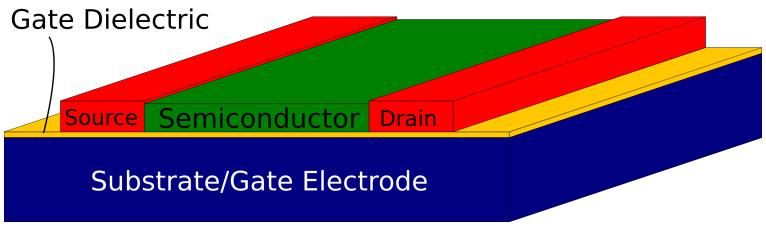


Figure 2.6.: Schematic of a back gate MOSFET with the source and drain electrodes in red, the gate dielectric in yellow, the semiconductor in green and the substrate/gate electrode in blue.

On a conductive substrate such as highly doped silicon, in most cases an insulating oxide layer like SiO_2 is prepared on top of the substrate acting as gate dielectric and the conductive substrate as gate electrode (see Figure 2.6). Silicon based metal oxide semiconductor MOSFETs are thereby mostly inversion mode devices. They are characterized by highly n-doped, metal like source and drain electrodes and a p-doped semiconductor connecting the two electrodes.

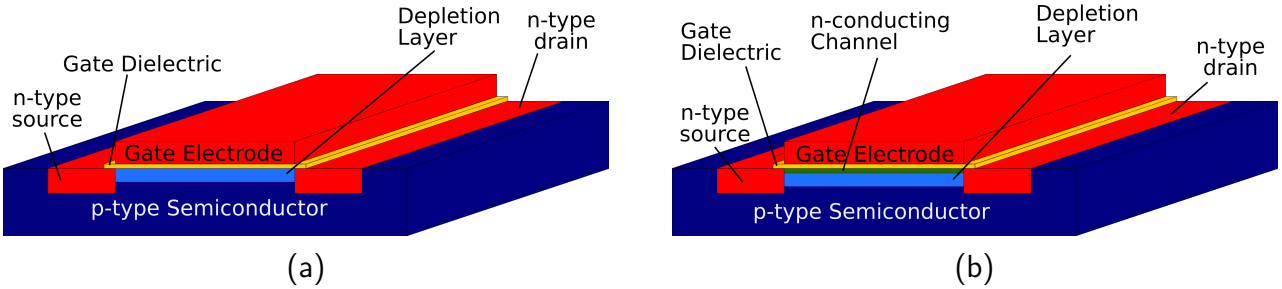


Figure 2.7.: Schematics of a top gate MOSFET with (a) $V_{gs}<V_{th}$ (depletion mode) and (b) $V_{gs}>V_{th}$ (inversion mode). Source and drain electrode are plotted in red, the gate dielectric in yellow, the depletion layer in light blue, the channel in green and the substrate in dark blue.

This n-p-n-structure ensures very low off currents due to the opposing p-n-junction on each side of the channel region. With application of a positive voltage at the gate, a depletion layer forms and with increasing V_{gs} an n-conducting channel develops at the semiconductor/dielectric interface (see Figure 2.7(b)). Such devices are called inversion mode FETs. Another type of transistor, which is actually used in this thesis, is the FET working in accumulation mode. Figure 2.8 shows the schematics of such an accumulation mode FET. In this case a poorly conducting n-type semiconductor is used as channel material between two likewise n-type source and drain electrodes.

By applying a positive voltage at the gate, the conductivity is increased and the device can be switched on.

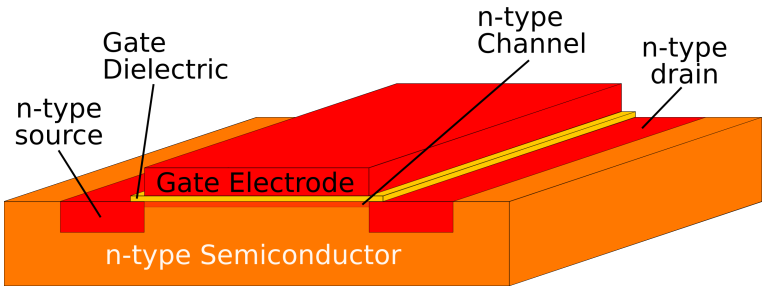


Figure 2.8.: Schematic of a top gate accumulation mode MOSFET with a voltage applied at the gate electrode $V_{gs}>V_{th}$. Electrodes (source, drain and gate) in red, gate dielectric in yellow, substrate in orange and channel in light red

Such an accumulation mode device has already been introduced for an in-plane device geometry by, e.g., Dasgupta et al. [2, 20, 22, 23]. In-plane FETs are gated with a liquid electrolyte solution or, as in the present thesis, by a composite solid polymer electrolyte (CSPE) to create an electric field at the semiconductor/electrolyte interface. The specialty of the electrolytes is that electrical double layers at the two spatially separated gate/electrolyte and electrolyte/semiconductor interface are formed. Further details are described in section 2.3. Three advantages of these electrolytes are, first that the generated capacitances are extremely high, second that they enclose the semiconductor very intimately even for very complex nanostructures and third electrolytes are easily printable. An example of such an electrolye gated FET is shown in Figure 2.9. Electrolyte gating allows for an ultimate field and gating effect.

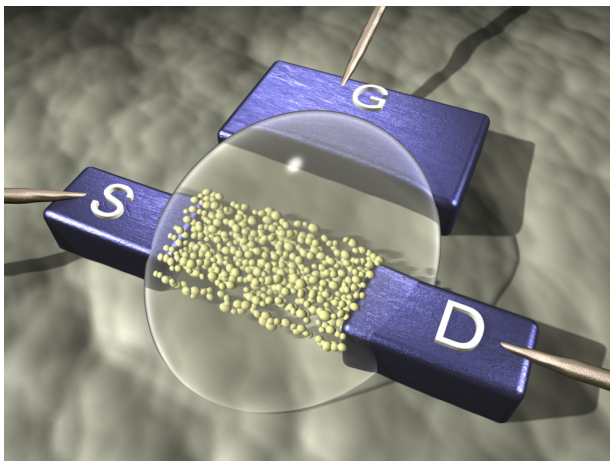


Figure 2.9.: Schematic of an electrolyte-gated, in-plane gate geometry FET with nanoparticulate channel material [22]

Figure 2.9 shows such a device with the electrodes all structured in the same plane, a nanoparticulate channel and electrolyte connecting channel and gate.

In 1986 a first report of a novel geometry for FETs was reported by Uchida et al. [63]. A vertical channel FET (v-FET) based on amorphous silicon technology was reported. The consequences of a rotated channel orientation can be a reduction of the channel length and a reduced lateral expansion. Miniaturizing these two geometrical factors enhanced the performance of silicon based FETs and was one of the driving forces for the progress of silicon technology in the last decades. Rotating the semiconductor in the transistor by 90 ° from a horizontal to a vertical direction is the easiest way to realize a v-FET and does not raise the need for new materials or technologies. However, using this approach, only the spatial extension is changed with the new device geometry. A more sophisticated approach of preparing a v-FET is the use of semiconducting nanowires as channel material (see Figure 2.10(a)). The nanowires are vertically aligned between source and drain electrode, which are located on top of each other. They get covered with a dielectric and a gate electrode, respectively, and create an array of single transistors, which can be addressed all together using a single gate electrode. Anyhow, this technique needs complicated and elaborate preparation techniques and is thus not of particular interest for mass production [64–66].

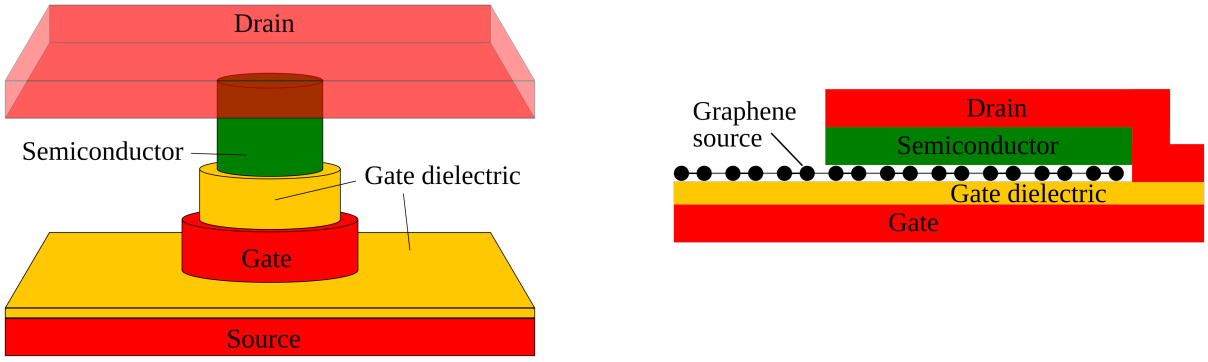


Figure 2.10.: (a) Schematic of a v-FET base on nanowires wrapped up in a dielectric and a gate electrode. (b) Schematic of a v-FET with a back gate geometry using graphene as penetrable source electrode.

A simpler way of preparing a vertically aligned channel geometry is to stack thin films in the right order (source/semiconductor/drain). The problem arising with this vertically aligned FET geometry is the gating. Using compact semiconductor materials, a gating is only possible at the edges of the channel. The result would be a ring channel geometry. To utilize the bulk semiconductor in between the drive electrodes, the field-effect needs to address the material in the middle of this ring as well. To achieve this, the gate electrode is placed underneath the channel region and is insulated with a dielectric. On top of it, a thin source (bottom) electrode is deposited, followed by the semiconductor and the drain electrode, subsequently. The electric field to turn

the semiconductor from insulating to conducting is then established between gate and drain. The thin source electrode can thereby be penetrated and does not hinder the field from developing. Such a source electrode can be made of, e.g., graphene (see Figure 2.10(b)) [67]. In this thesis a new porous semiconductor is introduced to prepare a novel v-FET that can be printed.

2.3 Electrolyte Gating

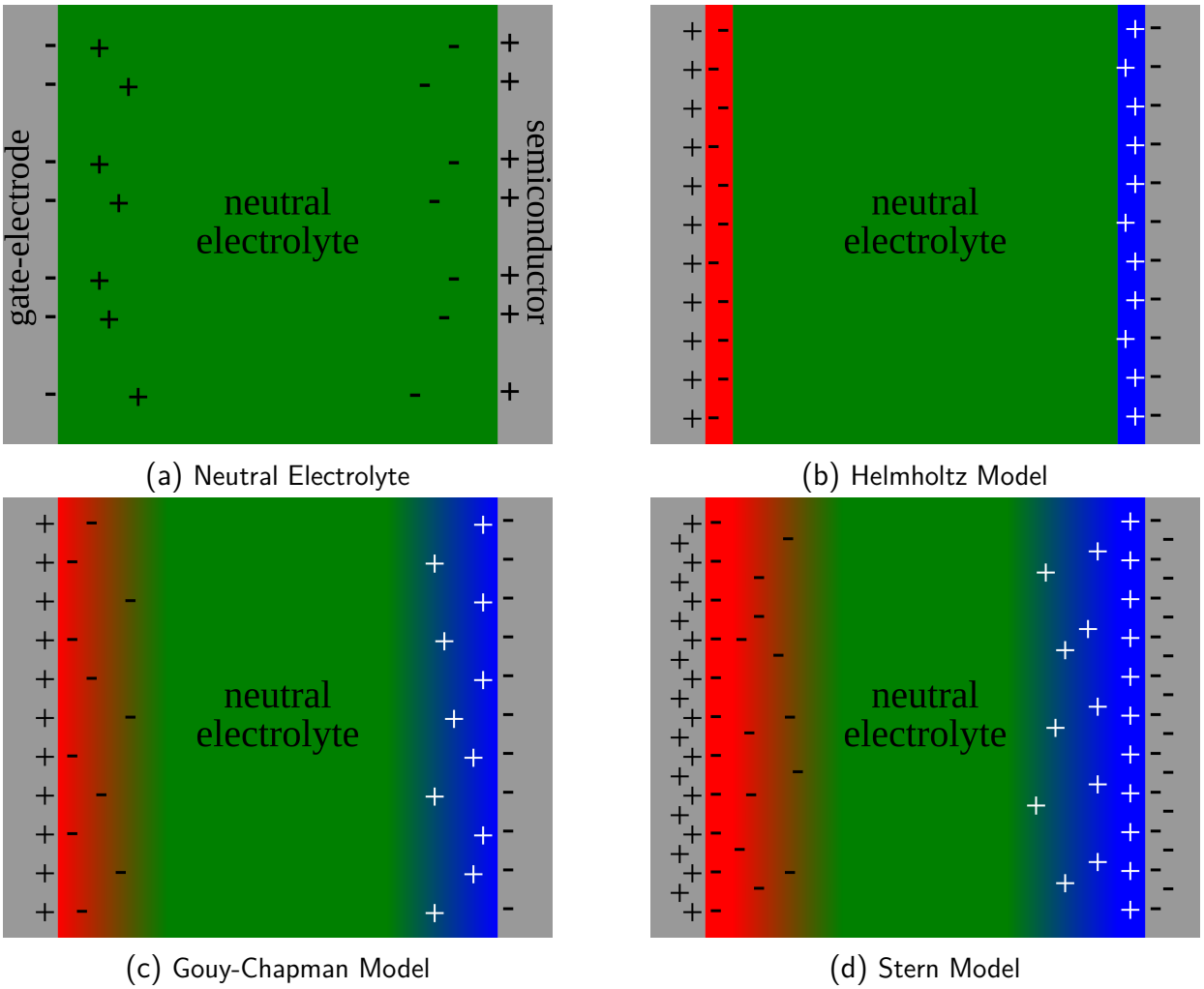
Electrolyte gating can be applied for in-plane gate geometry FETs, as well as porous channel FETs to contact the inner surfaces of the material. Following the general introduction of electrolytes, the specific demands to the electrolytes are discussed in section 2.3.2. Since the technique of electrolyte gating and its generalization to composite solid polymer electrolyte(CSPEs) gating is exclusively used throughout this thesis the mechanisms and processes occurring in the bulk of the electrolytes as well as close to the electrolyte/gate and electrolyte/semiconductor interfaces are described and some theoretical as well as application relevant considerations are made.

2.3.1 Liquid Electrolytes

For printed electronics, new gating approaches such as the use of electrolytes have been proposed [68–70] to overcome problems of printing soluble solidifying dielectrics with high dielectric constants on rough semiconductor surfaces. The utilized electrolytes are salts dissolved in polar solvents. The functional principle of such electrolytes is as follows: in the solvent the salt ions dissociate into anions and cations, which disperse homogeneously within the solution. If an electric field E is generated by means of an applied voltage or by a built-in potential between gate/electrolyte/semiconductor and source of an FET, the dissociated ions of the electrolyte experience the force $F = q \cdot E$ and drift towards the electrodes of opposite sign.

Schematic sketches of three different charge distributions after charge drift in the electric field E are shown in Figure 2.11. The first to realize the principal of charge pile up at the electrodes was Hermann von Helmholtz. He described in 1879 for the first time the existence of a layer of charges directly in touch or maximally divided by a solvation shell from the metal electrode carrying the opposing polarity charges. Helmholtz considered the electric double layer as a classical capacitor, only depending on the dielectric constant and the distance between electrode and ions. Louis G. Gouy and David L. Chapman in 1910 and 1913 made the observation that the magnitude of the areal capacitance was dependent on the applied voltage and included charge diffusion and intermixing with the electrolyte into their model. In their model the electric field decreases exponentially with distance from the electrode and thereby follows a Maxwell-Boltzmann distribution. Finally, in 1924 Otto Stern combined the two models and claimed that some ions actually approach the surface and form a Helmholtz double layer but some form a diffuse Gouy-Chapman layer. The latter model explains the functional principle of an electrolyte solution in contact with

two electrodes as it occurs in electrolyte-gated FETs (EG-FETs) and will be used in the present thesis.



(a) Neutral Electrolyte (b) Helmholtz Model

(c) Gouy-Chapman Model (d) Stern Model

Figure 2.11.: Schematics of an electrolyte solution in between a conducting and a semiconducting electrode: (a) without an applied field spurious charges may occur at the interfaces due to the different Fermi energies of metal and semiconductor, (b) presence of a Helmholtz double layer under an applied electric field, (c) presence of a diffuse double layer following the Gouy-Chapman model and (d) combination of (b) and (c) by the Stern model.

The most important effect of the charge separation in the electrolyte is the accumulation of charge within the electrolyte at the gate/electrolyte and the electrolyte/semiconductor interfaces, respectively. Thereby the accumulated ions are counterbalanced by charges in the metal gate and in the semiconductor. The so formed double layers of charges of opposite sign are called electrical double layers and establish a high areal capacitance due to the close proximity of the positive and negative charge carriers to the respective electrodes. The charges in the oxide semiconductor as used in this thesis are majority carriers, namely electrons, when a positive voltage is applied to the gate and vice versa for a negative voltage. In case of electrons the charges accumulate in a very narrow layer of the semiconductor facing the electrolyte whereas in case of the negative applied

voltage to the gate electrode, electrons are pushed out of the semiconductor into the source and drain contacts. This leaves behind a depletion layer of spatially fixed positively charged donors, which constitutes the reason why electrons are mobile and positive charges in form of ionized donors are immobile in this type of semiconductor. The high areal capacitance established by the electrical double layer is favorable for the FET since this allows to generate a high density of electrons for a small gate voltage. As mentioned before positive charges in the electrolyte thereby approach the electrons in the semiconductor at a distance comparable to the radius of the solvation shell surrounding the positive ions. The same configuration can be found at the gate/electrolyte interface where negative ions from the electrolyte are piled up at the metal gate at a distance comparable to the solvation shell surrounding the electrolyte ions. In between these two capacitors the electrolyte is almost free from the electric field and the bulk is therefore nearly electrically neutral (see Figure 2.11). It is still possible to conduct ions in the electrolyte since dissociation of the salt is still present. A simple electrical equivalent circuit of the situation is shown in Figure 2.12.

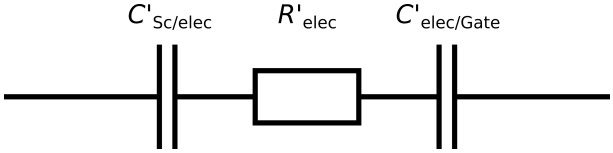


Figure 2.12.: Simple equivalent circuit of the gate/electrolyte/semiconductor system as a representative of an EG-FET.

The equivalent circuit consists of two capacitances and a connecting resistor. The total capacitance C'_{tot} is thereby the series connection of the capacitance $C'_{\mathrm{Sc/elec}}$ of the semiconductor/electrolyte interface and of the capacitance $C'_{\mathrm{elec/gate}}$ of the electrolyte/gate interface as displayed in eq. (2.13):

$$\frac{1}{C'_{\mathrm{tot}}} = \frac{1}{C'_{\mathrm{Sc/elec}}} + \frac{1}{C'_{\mathrm{elec/Gate}}} \tag{2.13}$$

The electric field in the electrolyte after charge separation is no longer uniform. It is very high in the interface regions and very low in the remaining bulk of the electrolyte. Due to the charge separation it is possible to generate a very high electric field with relatively small voltages. It is even possible to enhance the electric field by using a gate electrode area, which is much bigger than the actual gated semiconductor area. In this case $C'_{\mathrm{elec/gate}}$ is becoming much bigger than $C'_{\mathrm{Sc/elec}}$ and the voltage drop is not equally shared between the two capacitors but drops almost exclusively across $C'_{\mathrm{Sc/elec}}$. This can result in an increase of the electric field by almost a factor of two, which is a great improvement because of the electric field leading to charges being pulled into the transistor channel.

The ohmic nature of the resistance R_{elec} can be understood by the fact that the specific conductivity σ_{el}

$$\sigma_{\text{el}} = e(n_{\text{ion}^+}\mu_{\text{ion}^+} + n_{\text{ion}^-}\mu_{\text{ion}^-}) \tag{2.14}$$

is constant and the bulk stays electrically neutral so no space charge accumulates and causes space charge effects like nonlinear resistances. The neutrality requires that the local charge densities n_{ion^+} and n_{ion^-} are equal in the bulk. This requirement is fulfilled, since the salt is completely dissolved. The ion mobilities μ_{ion^+} and μ_{ion^-} are also constant and are known from literature to range between $9{\cdot}10^{-4}\,\text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$ and $1.8{\cdot}10^{-2}\,\text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$ [71]. An estimate of the resistance R_{elec} can then be performed by introducing the geometrical parameters. It yields

$$R_{\text{elec}} = \frac{1}{\sigma_{\text{el}}}\frac{L}{A} \tag{2.15}$$

where L is the length and A the area of the resistor. Knowing R_{elec} and C'_{tot} one can determine the actual charging time τ of the transistor, which is given by the Maxwell relaxation time. The relation is described in eq. (2.16)

$$\tau = \epsilon \cdot \frac{\epsilon_0}{\sigma_{\text{el}}} = R_{\text{elec}} \cdot C'_{\text{tot}} \tag{2.16}$$

This equation holds only, if other time constants like the one for charging the channel are much smaller than the Maxwell relaxation time τ. The electric field created by the Helmholtz and Gouy-Chapman double layer can reach values up to $10\,\text{MV}\,\text{cm}^{-2}$ on a distance of a few nanometers. This distance is determined by the solvation shell, which defines the distance between electrode/channel and ions. This corresponds to an areal capacitance of $1\text{-}10\,\mu\text{F}\,\text{cm}^{-2}$. Besides generating such large capacitances $C'_{\text{Sc/elec}}$ at the semiconductor/electrolyte interface further advantages of electrolyte gating should be mentioned. First of all the involved solutions are easily printable and secondly the solutions are particle free and therefore adapt exactly to the surface roughness of the printed semiconductor. This implies that the interface quality of the semiconductor does not play a role with printed electrolyte films at all, as long as the electrolyte can contact the semiconductor surfaces. Furthermore, the choice of substrate is not an issue for the electrolytes in printed electronics anymore. Electrolytes can be processed at room temperature and do not need high temperatures to form good interfaces as for example oxide dielectrics. Therefore, the need to use rigid and temperature stable substrates like glass or silicon is not given anymore. Electrolytes can be processed on flexible substrates like PEN or PET, which also qualify for high throughput roll-to-roll processes.

2.3.2 Composite Solid Polymer Electrolyte

Since the liquid state of the electrolyte is not really suitable for application in daily use, solidification of liquid electrolytes is necessary without loosing the functionality. Different approaches have been suggested so far, i.e., the use of solid polymer electrolytes [72], ionic gels [73] and composite solid polymer electrolytes [20, 22, 23]. All these materials are based on liquid electrolytes mixed with polymers like polyvinyl alcohol (PVA) or polyethylene oxide (PEO) ensuring a solid matrix for the electrolyte. Consequently, the polymer has to be chosen in such a way that the ion mobility is still sufficiently large in the solid state. Furthermore, the solution has to be printable, meaning soluble, and manageable at ambient conditions. Ion gels, as the solid equivalent of ionic liquids are moisture sensitive and degrade under ambient conditions quickly and solid polymer electrolytes usually suffer from poor ionic conductivity (see appendix, table E.1). The composite solid polymer electrolyte on the other hand preserves the high ionic conductivity of the liquid electrolyte because the solvents are chosen such, that they do not evaporate entirely and thus enables a fast ion movement even in a "quasi" solid state.

To make the material printable a solvent has to be added to reduce the viscosity to a value where the material meets the requirements of the inkjet printer. An ink with good printability usually has a surface tension of 10 - 20 cP and a viscosity of 10 - 50 $\mathrm{mN\,m^{-1}}$. The CSPE solution with values in this range is then printed in a liquid state and solidifies during the evaporation of the solvent. The liquid application creates a conformal gate/electrolyte and electrode/semiconductor interface. This interface quality is necessary to ensure a homogeneous formation of the electrical double layer as described before.

3 Experimental

3.1 Material and Device Characterization Methods

In the following section, the characterization methods used in this thesis are presented. Chemical, mechanical and imaging techniques are introduced and the electrical device characterization is discussed in detail.

3.1.1 Differential Scanning Calorimetry

In order to study the phase transition of the remaining liquid in the investigated composite solid polymer electrolytes (CSPEs) the technique of differential scanning calorimetry (DSC) is used. It is a thermoanalytic technique and is used to measure the change in the heat capacity of the sample during heating and cooling. The samples have therefore been heated up and cooled down linearly together with a standard reference such that both are kept at the same temperature. The necessary energy to maintain the identical temperature is recorded. If the heat capacity of the reference is known, the one of the investigated sample can be determined. In case of change in state of aggregation, the heat capacity versus temperature diagram exhibits characteristic features, which can be assigned to endothermic and exothermic processes, which then reflect certain phase transition like a crystallization or the occurrence of a glass transition. The measurements are performed using the DSC 30 from Mettler Toledo equipped with a patented DSC sensor with 120 thermocouples guaranteeing very high sensitivity. Measurements are performed in a temperature range between -100 °C and 25 °C with a ramping speed of 10 °C min^{-1}.

3.1.2 Micro-Tensile Testing

Tensile testing is used in this thesis to determine the mechanical properties by means of stress/strain behavior of CSPE samples. Thereby a sample is stretched with a certain rate and the stress is recorded until mechanical failure occurs. Stress and strain are thereby defined as follows:

$$\text{Strain:} \qquad \epsilon_{\mathrm{st}} = \frac{\Delta L_{\mathrm{st}}}{L_{\mathrm{st},0}} = \frac{L_{\mathrm{st}} - L_{\mathrm{st},0}}{L_{\mathrm{st},0}} \tag{3.1}$$

$$\text{Stress:} \qquad \sigma_{\mathrm{st}} = \frac{F_{\mathrm{n}}}{A} \tag{3.2}$$

where L_{st} is the length under stress, $L_{st,0}$ the initial length of the sample, F_n the tensile force in normal direction to A, which is the cross section of the sample.

In the present study 16 mm×10 mm dried CSPE strips are mounted in the micro tensile testing machine from Kammrath and Weiss GmbH, Dortmund designed to perform load experiments on small samples. The films are clamped into one static and one movable jaw covering 4 mm of the sample length each. At the beginning of the experiment the distance between these two clamps is accordingly fixed to 8 mm and a pulling speed of 10 μm s^{-1} is utilized to stretch the sample. The tensile stress is recorded by means of a force gauge and plotted with respect to strain.

3.1.3 Rheology

Rheology measurements are performed for to CSPEs to understand the solidification process and the temperature dependent viscosity of the dried material. The liquid CSPE is mounted between two plates, which are rotated against each other. The measured properties are the storage modulus and the loss modulus, which basically indicates how much of the energy put into the system via rotation is stored and regained during relaxation. The difference is the lost energy due to deformation or heat development. By analyzing these quantities it is possible to make a conclusion about the viscoelastic state of the CSPE. In the dried state of the CSPE the technique is also suited to investigate the temperature dependence of the storage and loss modulus.

The shear modulus measurements are performed in the Compact Modular Rheometer MCR 501 from Anton-Paar. To determine the temperature dependence of the moduli one plate of the rheometer is exchanged by another plate combined with a Peltier element of a diameter of 8 mm (PP08/TG). The gap is 0.05 mm and is automatically adjusted and controlled during the experiment to maintain zero normal force on the sample. The rotation amplitude is 0.1 % of the gap and the angular frequency is 1 rad s^{-1}.

3.1.4 Scanning Electron Microscopy

To investigate the morphology of the porous structure of SnO_2 scanning electron microscopy (SEM) is used. To generate the image of the structure the SEM uses a focused electron beam with energies between 1 and 30 kV, which is scanned across the sample. The electron beam thereby interacts locally with the sample in high vacuum producing secondary electrons, Auger electrons, backscattered electrons and characteristic X-rays (see Figure 3.1). The intensity of one of the secondary species (in the present case those of the secondary electrons) is recorded simultaneously with the location of the focus of the electron beam and thus generates a high spatial resolution image. The spatial resolution is limited to the size of the ionized volume, which can be as small as 1 nm in diameter.

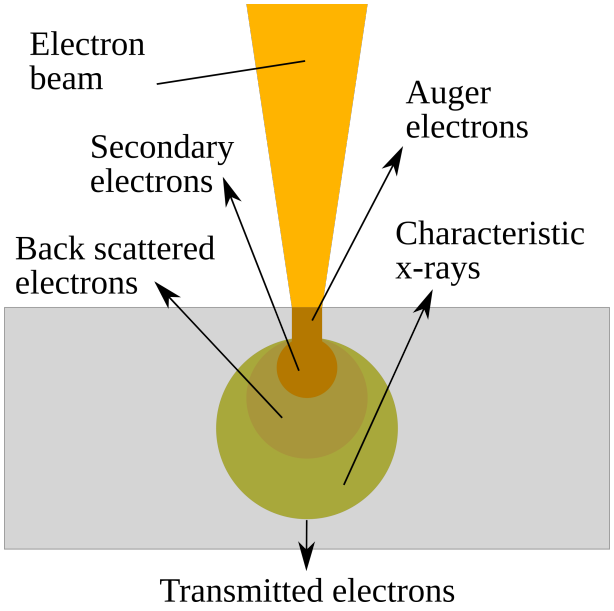


Figure 3.1.: Schematics of the interaction between a focused electron beam and sample. From the interaction volume different secondary species are emitted as indicated.

SEM analysis can be performed on all kinds of solids. For soft matter and insulating materials, a thin layer of a conductive coating like gold or carbon, has to be applied to avoid charging effects and ensure structural integrity. The utilized scanning electron microscope is the Model Leo1530 from Zeiss Jena.

3.1.5 Transmission Electron Microscopy

In this study transmission electron microscopy (TEM) is used to investigate the crystallinity of porous SnO_2 as used in the semiconductor structure of the vertical field-effect transistor. Therefore very thin slices of the SnO_2 have to be prepared ($< 100\,\text{nm}$) in order to be penetrated by the high energy electron beam with energies of up to 300 kV. The penetrating electrons interact with the atoms of the sample by means of elastic and inelastic scattering processes. The transmitted beam then contains information about the crystal structure, crystal composition, etc. The resolution, depending on the sample preparation, can be as high as 0.5 Å, which allows for the analysis of the crystal lattice (crystal structure, defects, etc.) on the atomic scale. The utilized transmission electron microscope is an aberration (image) corrected Titan 80-300 TEM from FEI Company operated at an acceleration voltage of 300 kV. It is equipped with an US1000 slow scan CCD camera from Gatan, Inc. for TEM imaging and a high angle annular dark field detector from Fischione Instruments for scanning TEM (STEM) imaging.

3.1.6 Electron Tomography

To determine the porosity of the SnO_2 the technique of electron tomography is employed. It uses the TEM technique allowing for the construction of high resolution three dimensional images. In electron tomography the sample is now rotated around one axis and images are taken at increment angles. These individual images are used afterwards to mathematically reconstruct a 3D image. The utilized TEM is the same as described in section 3.1.5.

3.1.7 Impedance Spectroscopy

In the present thesis the technique of impedance spectroscopy is used with the goal to determine the electrical properties of the investigated CSPEs and to find an equivalent circuit, which is able to describe the measured data correctly. Thereby impedance spectroscopy is a noninvasive technique, in which the electrical response to an applied AC voltage $V(t)$ to the actual sample is measured and evaluated in terms of an electrical equivalent circuit. The applied sinusoidal signal, when represented by a complex valued function, can be written in form of the following equation

$$V(t) = |V_0|e^{i(\omega t)} \tag{3.3}$$

where V_0 is the amplitude of the signal and ω the angular frequency. The response signal $I(t)$ with the amplitude I_0 is shifted by a phase angle φ and is represented by

$$I(t) = |I_0|e^{i(\omega t+\varphi)} \tag{3.4}$$

From the applied voltage $V(t)$ and the response current $I(t)$ the impedance can be stated in analogy to Ohm's law as follows:

$$Z = \frac{V(t)}{I(t)} = \frac{|V_0|e^{i(\omega t)}}{|I_0|e^{i(\omega t+\varphi)}} = |Z|e^{-i\varphi} \tag{3.5}$$

Thus the impedance is defined in terms of the absolute value $|Z| = \frac{|V_0|}{|I_0|}$ and the phase angle φ.

The acquired raw data can be plotted in two different ways: (1) as Bode plots, which show $|Z|$ and φ with respect to the frequency f and (2) as a Nyquist plot, which shows the imaginary part of the impedance Z'' with respect to the real part Z'. Figure 3.2(a) and 3.2(b) show typical Bode plots whereas Figure 3.2(c) displays a typical Nyquist plot.

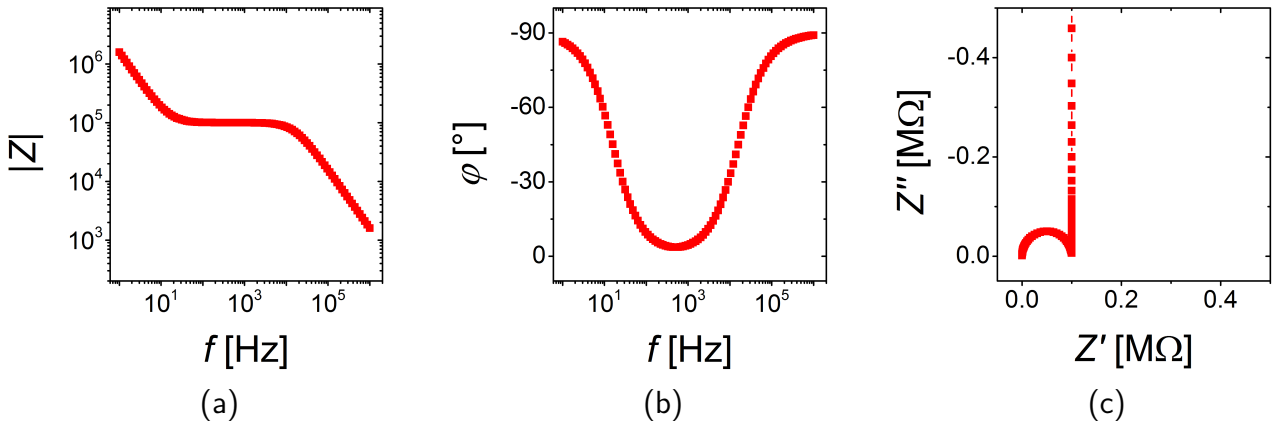


Figure 3.2.: Exemplary Bode plots (a) and (b) and Nyquist Plot (c).

For analysis, an equivalent circuit is developed. Every component of this equivalent circuit represents a physical process in the measuring setup. Figure 3.3 displays exemplarily the equivalent circuit, which represents the data shown in Figure 3.2.

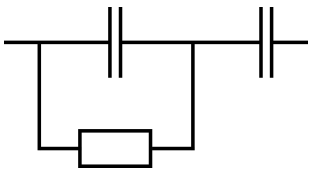


Figure 3.3.: Equivalent circuit of a simple electronic system consisting of two capacitors and one resistor.

The impedance measurements are conducted with a Biologic SP-150 Value Oriented Research Grade Electrochemical Impedance Spectrometer with capabilities for potentiostatic/galvanostatic measurements in the frequency range from 1 Hz to 1 MHz. An AC voltage amplitude of $V_{\mathrm{ac}} = 5\,\mathrm{mV}$ is applied. The system measures at 15 frequencies per decade and averages over 50 measurements for each frequency. Due to a large physical distance between the impedance spectrometer and the measuring cell relatively long cables had to be used to connect to the sample.

3.1.8 Electrical Characterization of FET

Since the main topic of this thesis is the fabrication and characterization of electrolyte-gated field-effect transistors the methods for the determination of the most important performance parameters are highlighted. The Shockley equations 2.9 and 2.10 as displayed in section 2 serve as the theoretical basis.

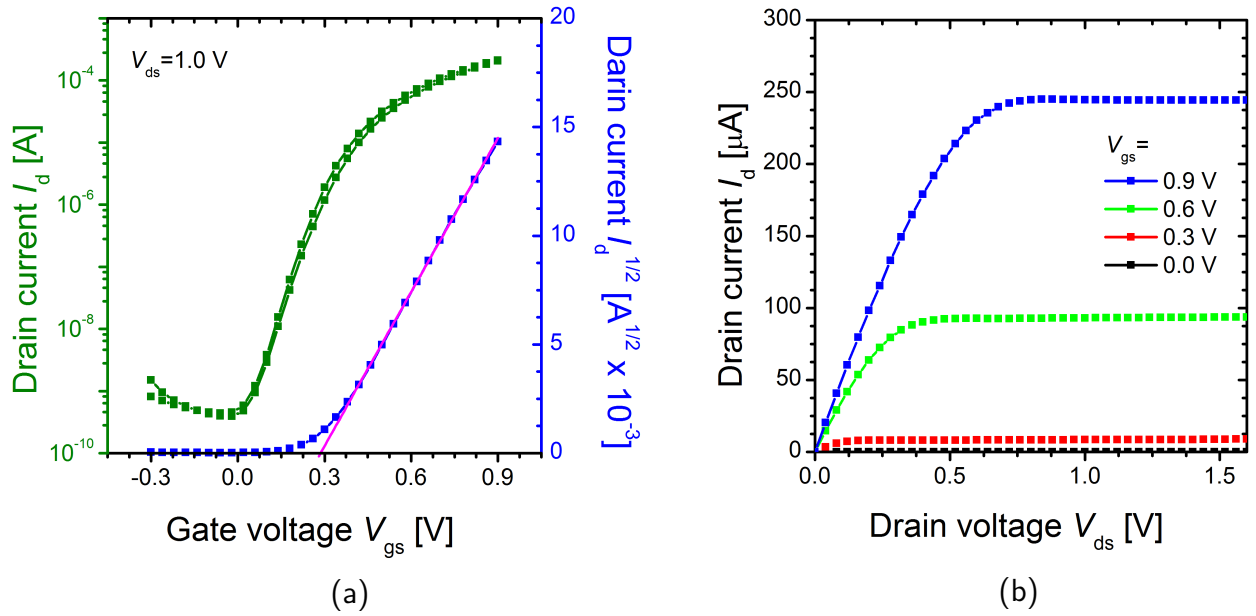


Figure 3.4.: Transistor characteristics of an in-plane electrolyte-gated printed FET measured at 30 °C. (a) transfer characteristics (green) and the $\sqrt{I_d}$ curve (blue) and (b) output characteristics for different gate voltages V_{gs}.

The transfer and output curves are analyzed and the characteristic device properties such as off-current, on-current, on/off-current ratio, subthreshold swing, threshold voltage and field-effect mobility are extracted from the two characteristics as exemplarily shown in Figure 3.4 in the following way:

- The on/off-current ratio is determined from the current difference of the drain current I_d at gate voltage $V_{gs} = 0.0\,V$ and $V_{gs} = 0.9\,V$. On- and off-currents are consequently extracted at the current values of the respective V_{gs} values.

- The subthreshold swing SS is determined from the slope of the logarithmic transfer curve (green) between $V_{gs} = 0.0\,V$ and the threshold voltage V_{th}.

- The threshold voltage V_{th} is taken from the linear regression line of the ${I_d}^{1/2}$ curve (blue) extrapolated towards ${I_d}^{1/2} = 0$. V_{gs} at the intersection of the ${I_d}^{1/2}$ with the V_{gs} axis is defined as V_{th}. This procedure can be understood theoretically by eq. (3.6) since for $V_{ds} = V_{th}$ the linear regression line of the current ${I_d}^{1/2}$ becomes 0.

- The field-effect mobility μ_{FET} is determined using the slope of the linear section of the ${I_d}^{1/2}$ curve. Utilizing eq. (2.10) for the saturated on-current. One obtains:

$$I_{d,sat}^{1/2} = \sqrt{\frac{W}{2L}\,\mu_{FET}\,C_{dl}} \cdot (V_{gs} - V_{th}). \tag{3.6}$$

where W is the channel width, L the channel length and C_{dl} the areal double layer capacitance. The other variables assume their usual meaning. The square root term can then be interpreted as the slope a of the mean straight line, which can be determined experimentally.

$$a = \sqrt{\frac{W}{2L}\,\mu_{\mathrm{FET}}\,C_{\mathrm{dl}}} \tag{3.7}$$

With the measured slope and known areal capacitance from the impedance spectroscopy [20] μ_{FET} can be calculated to

$$\mu_{\mathrm{FET}} = \frac{2L\,a^2}{W\,C_{\mathrm{dl}}}. \tag{3.8}$$

This formula is much more robust than taking directly eq. (2.10) and utilizing a single data point because the square root approach relies on multiple data points and already averages out experimental data fluctuations. Additionally, the formula does not depend on the precise determination of V_{th}. The areal double layer capacitance of an In_2O_3/electrolyte interface has been measured by Garlapati et al. [20] with a similar setup as the parallel plate capacitor described. In their setup the In_2O_3 electrode was much smaller than the ITO counter electrode and their measured areal capacitance was $4.3\,\mu\mathrm{F\,cm^{-2}}$ at room temperature. In the present study we assume the value measured by Garlapati et al. [20] and utilize the temperature dependence of the here measured ITO/CSPE areal double layer capacitance.

The characteristics of the FETs, which are prepared as described later in section 3.3.6 and measured at room temperature, are analyzed using an Agilent 4156C Semiconductor Parameter Analyzer connected to a MicroSüss probe station via triaxial cables. The three electrical probes are equipped with tungsten needles for contacting the transistor. For the temperature dependent measurements of the sealed FETs as described in section 3.3.6 the three aluminum strips are attached to triaxial cables. For all FETs, transfer and output characteristics are recorded for different gate and drain voltages, respectively. The voltage range is chosen carefully to display all FET properties and allow extracting all characteristic values of the FETs. The sweep of gate and drain voltage is conducted with no time delay between voltage steps if not stated otherwise. For all measurements drain and gate voltages as well as drain, source and gate currents have been recorded simultaneously for subsequent data analysis.

3.2 Ink Preparation

In this section the fabrication of different solutions for printing is described. Ingredients are stated and the exact preparation routines are presented.

3.2.1 Indium Oxide Precursors

The precursor ink for the semiconducting In_2O_3 thin film channels is prepared by dissolving $In(NO_3)_3$ salt in double distilled water. For better drying and printing behavior the solution was mixed with glycerol. The final composition is a 0.05 molar solution containing 0.15 g $In(NO_3)_3$ (99.99 %, Sigma Aldrich), 8 g of double distilled (dd) water and 2 g glycerol (99.5 %, Merck Millipore)(Figure 3.5).

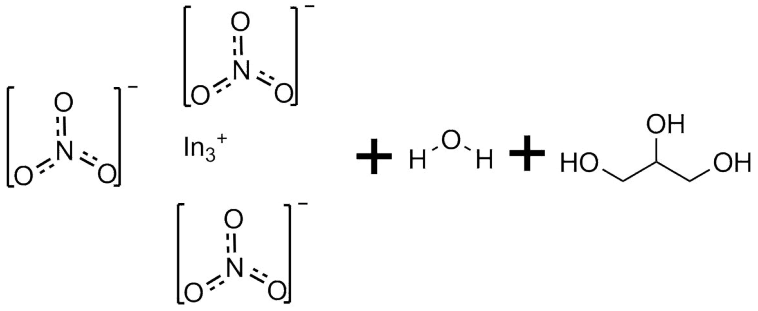


Figure 3.5.: Ingredients of the In_2O_3 precursor solution utilizing a weight ratio of $In(NO_3)_3$: double distilled H_2O : Glycerol = 0.15 : 8 : 2

After mixing, the solution is stirred with a magnetic stirrer with 300 rpm at room temperature until the solution turns transparent. To finalize the process, the solution is filtered through a 0.2 μm polytetrafluoroethylene (PTFE, GE Healthcare) filter to remove undissolved starting materials. The so prepared solution can be printed as prepared.

3.2.2 Tin Oxide Precursors

A SnO_2 precursor ink has been developed to print a porous semiconductor layer. The ink is fabricated, following the route of Brezesinski et al.[74]: first, a homogeneous solution is prepared by dissolving 285.5 mg $SnCl_4$ and 75 mg of poly(ethylene-co-buthylene)-block-poly(ethylene oxide) (referred to as KLE) in 3.2 ml of ethanol (absolute 99.5 %, Merck Millipore). Subsequently, after adding 0.3 ml of water under stirring to catalyze the hydrolysis reaction, the resultant mixture is aged for about 24 h before it was used for printing.

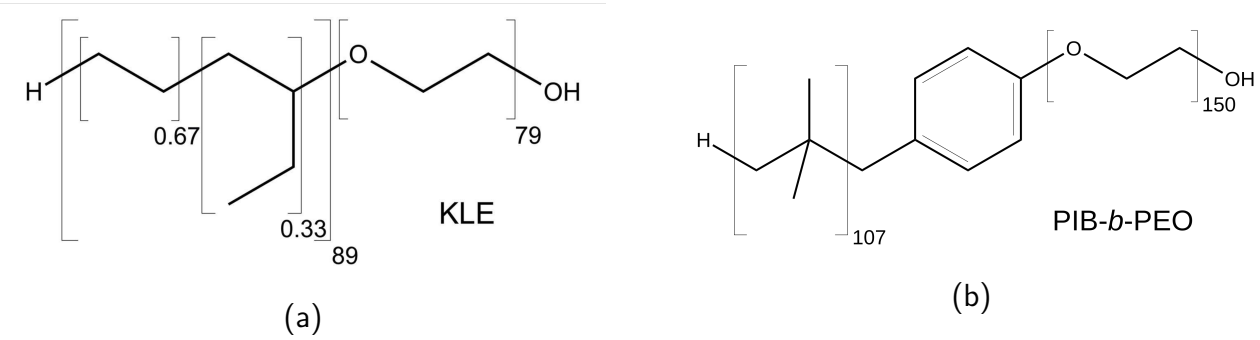


Figure 3.6.: Chemical structure of two block-copolymers used for preparation of porous SnO_2 films: (a) poly(ethylene-co-buthylene)- block-poly(ethylene oxide) and (b) poly(isobuthylene)-block-poly(ethylene oxide)

The entire process is carried out at ambient conditions. A second solution was prepared using poly(isobutylene)-block-poly(ethylene oxide) (PIB-b-PEO) as a micelles forming polymer. All other ingredients were kept the same. Figure 3.6 shows a schematic structural chemical formula of the two used block-co-polymers.

3.2.3 Composite Solid Polymer Electrolytes

The composite solid polymer electrolytes (CSPEs) are prepared from lithium perchlorate ($LiClO_4$, 99.99 %, Sigma Aldrich GmbH) and propylene carbonate (PC anhydrous 99.7 %, Sigma Aldrich GmbH), which are mixed in a mass ratio of 1 : 9 in a sealed glass vessel and stirred at room temperature until a transparent solution is obtained. In a different vessel, polyvinyl alcohol (PVA, hydrolyzed 98 %, Sigma Aldrich GmbH) and dimethyl sulfoxide (DMSO, anhydrous 99.9 %, Sigma Aldrich GmbH) are mixed at a mass ratio of 1 : 10 at 50 °C for 12 h. All chemicals are used without further purification. Finally, the first solution is slowly poured into the second one under continuous stirring up to a mass ratio of 7 : 30, while the vessel is placed on a hot plate at 50 °C. The final solution (CSPE-1) after turning completely transparent and homogeneous, is filtered through a 0.2 μm (PTFE, GE-Healthcare) filter. In an analogue way, two more electrolytes have been prepared with PC substituted by mixtures of PC : DEC ($\geq$ 99 %, Sigma Aldrich GmbH) (1 : 1) and PC : EMC (99 %, Sigma Aldrich GmbH) (1 : 1) (CSPE-2 and -3). Figure 3.7 displays a schematic diagram of the structural chemical formula of the utilized compounds and compositions.

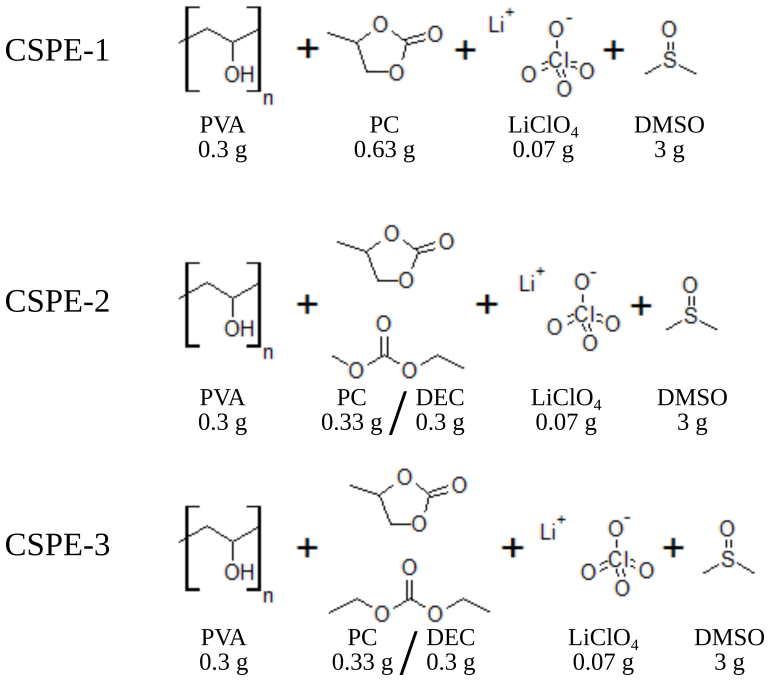


Figure 3.7.: Ingredients and composition of three analyzed CSPEs.

3.3 Device Preparation

In the following section the preparation routines of the samples used for mechanical and chemical testing as well as the fabrication of devices for electrical characterization throughout this thesis are presented.

3.3.1 Samples for Mechanical Testing

To investigate the mechanical properties of the CSPEs samples are prepared as solid films produced by controlled solvent evaporation from the liquid mixtures filled in petri dishes. After several days under ambient conditions a transparent rubber like film has formed, which was used after showing constant weight for the following 3 days. At this point the samples are considered to be in a stable state. For tensile stress measurements a $16\,mm \times 10\,mm$ piece was cut out of the rubber like film.

The samples for rheology measurements were prepared by infiltrating the liquid CSPE in between the plates of the rheometer under constant flow of $200\,\mathrm{l\,min^{-1}}$ of dry air. In order to keep the measuring conditions constant with time the normal force was set to zero so that a volume reduction would not cause a detaching of the sample. After a solidification period of 60 h the experiments indicated constant properties and the samples were considered to be stable.

Differential scanning calorimetry samples have been prepared in aluminum boats by drying the liquid CSPE solution until a constant weight was reached. After solidification, the sample was sealed hermetically to ensure no mass loss for the duration of the experiment.

3.3.2 Laser Ablation

For the preparation of passive electrode structures a laser ablation technique has been used, which utilizes a pulsed infrared (IR) laser (Trumpf, TruMicro 5050) with a wavelength of 1030 nm, a pulse length of < 10 ps and a maximum pulse energy of 250 μJ. The pulse frequency is set to 800 kHz with a mean power of 50 W. With an optical setup for precision scanning an ablation width of $\sim$20 μm is achieved with a positioning accuracy of 5 μm. The mechanism of this technique is cold ablation. It is based on the effect, that energy, deposited by the laser light is rapidly re-emitted by means of ionized atoms.

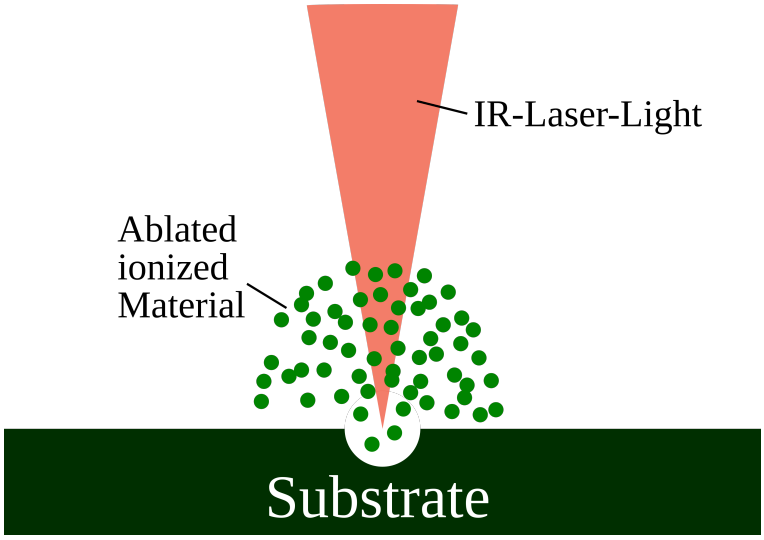


Figure 3.8.: Schematic of a Coulomb explosion after local ionization due to an IR laser pulse irradiation.

The ablation works on the principle of Coulomb explosion. The highly focused laser pulse ionizes many atoms in a defined area and the electrostatic Coulomb force causes repulsion of the ions from each another. This resulting force is strong enough to break atomic bonds in the solid and thus evaporates the ionized species in the exposed area. In this way the deposited energy has no time to convert into heat, which would dissipate into the substrate. Figure 3.8 shows a schematic of the process.

3.3.3 Electron Beam Lithography

Electron beam lithography is used to structure the electrodes of the vertical FET (v-FET) to be introduced in section 5. For the lithographic structuring of the gate and source on a substrate of

Si/SiO_2 poly(methyl methacrylate) (PMMA 950K, Allresist) as an energy sensitive resist is deposited by spin coating with 8000 rpm for 60 s followed by an annealing step at 160 °C for 30 min. The resulting 180 nm PMMA is exposed to 30 keV electrons using a Raith Elphy Plus pattern processor system attached to the above mentioned scanning electron microscope Model Leo1530 from Zeiss Jena.

Figure 3.9.: Schematics of the process of electron beam lithography showing a PMMA covered substrate (left), a structured PMMA covered substrate with exposed regions after electron irradiation and developing (middle) and the final structures made of platinum by sputter deposition and lift off technique (right)

The irradiated portion of the resist is removed in a 1 : 3 mixture of MIBK[1] and Isopropanol, which leaves the non-irradiated PMMA unaffected. This PMMA mask is now used to deposit platinum or the material of choice on top of the remaining resist and into the exposed regions. The final lift-off process is performed in acetone in an ultrasonic bath, which removes the excessive resist with the Pt on it, leaving the Pt in the exposed regions unaffected. Figure 3.9 shows a schematic of the process.

3.3.4 Inkjet Printing

For device preparation on laboratory scale a flexible and precise printing technique is indispensable. The chance to quickly change designs is a prerequisite for a fast progress and development. A precise deposition of the printed materials and thus a high resolution is of utmost importance for reproducible device fabrication. An inkjet printer as shown in Figure 3.10, provides these features as a digital printing technique with a resolution of $\sim$20 μm and a deposition accuracy of $\sim$5 μm. An inkjet printer consists of a stage to place the substrate and a printhead where the nozzles are located. The ink is stored in a reservoir that is connected to the nozzles. Piezoelectric crystals in the nozzles oscillate with a base frequency and amplitude to keep the liquid in motion and avoid drying at the orifices. In this state the amplitude is not big enough to form and eject a droplet. If a droplet is wanted to be ejected an additional electrical pulse with a certain wave function and phase angle has to be applied to the piezoelectric crystal in order to force the droplet to form and leave the nozzle. The distance between printhead and substrate can be adjusted in the range of 0.1 mm to 2 mm depending on the substrate structure and the drop formation. After leaving the

[1] methyl isobutyl ketone

nozzle it takes a while for the droplet to reach a stable shape. The utilized distance to achieve such a stable shape is the minimum gap between nozzles and substrate required to maintain good and stable printing conditions.

Figure 3.10.: Picture of a Dimatix 2831 desktop inkjet printer as used throughout this thesis.

The size of the droplets on the substrate depends on the interaction between substrate and ink. The Figure of merit describing the behavior of a liquid on a surface is the contact angle Θ and the surface energies of the liquid σ_L, the solid σ_S and the interface liquid/solid σ_{LS}. The relation between the contact angle to the surface tensions is described by Young's formula

$$\Theta = \cos^{-1}\left(\frac{\sigma_S - \sigma_{LS}}{\sigma_L}\right) \tag{3.9}$$

One can see that a decrease of σ_S corresponds to a decrease in contact angle and vice versa for σ_L. With a larger contact angle the same amount of liquid is occupying less space on the substrate, which results in a smaller droplet size. The surface tensions can be influenced by surface treatments with oxygen plasma or chemicals to increase σ_L or the addition of polymers to the liquid solution to reduce σ_S. By this means the ink/surface interaction can be influenced. Independent of the interaction of droplet and substrate, the size of the droplets can be controlled by the voltage pulse shape and magnitude applied to the piezoelectric crystal. The higher the applied voltage, the more ink is ejected from the nozzle orifice and the higher escape velocity is reached. As a consequence the diameter of the droplet on the substrate increases.

There are also problems with inkjet printing, which should be mentioned. The common ones are clogging of the nozzles, a related change of droplet shape and direction of motion and

the appearance of satellite drops. The consequence of a high viscosity solvent can be a failed drop formation after all. A low boiling point and high vapor pressure of the solvent can lead to excessive evaporation of the solvent leaving unresolvable remains, e.g., nanoparticles at the orifice. In nanoparticulate dispersions, agglomeration can occur due to poor or no stabilization of the nanoparticles in the solvent and can cause clogging of the nozzles. For primary particles the rule is that the ratio between the orifice of the nozzle and the diameter of particles should be at least 100:1. A change in drop forming behavior and the formation of satellite droplets is caused by remains of clogged nanoparticles at the nozzle orifice. To avoid this phenomena the surface tension of the nozzle material and the ink have to be well adjusted.

The printing of channel materials and CSPEs is performed using a commercial Dimatix 2831 desktop inkjet printer (see Figure 3.10). The distance between printhead and substrate is chosen in a way that a good drop formation is ensured ($\sim 400\,\mu$m). The jetting frequency is set to 5 kHz and the drop spacing is adjusted to fit the requirements of the respective application. The jetting voltage is between 25 V and 40 V depending on the viscosity and geometric requirements of the film to be deposited. Before printing a cleaning of the nozzles is performed ensuring a good and reliable drop ejection and formation.

3.3.5 Fabrication of Parallel Plate Capacitors

In order to measure the electrical properties of the CSPE by impedance spectroscopy a parallel plate capacitor is fabricated. The electrodes are prepared by laser ablation starting from ITO coated glass substrates. The capacitor is constructed by two glass slides with laser structured ITO electrodes of $2 \times 1\,\text{mm}^2$ facing each other as shown in Figure 3.11.

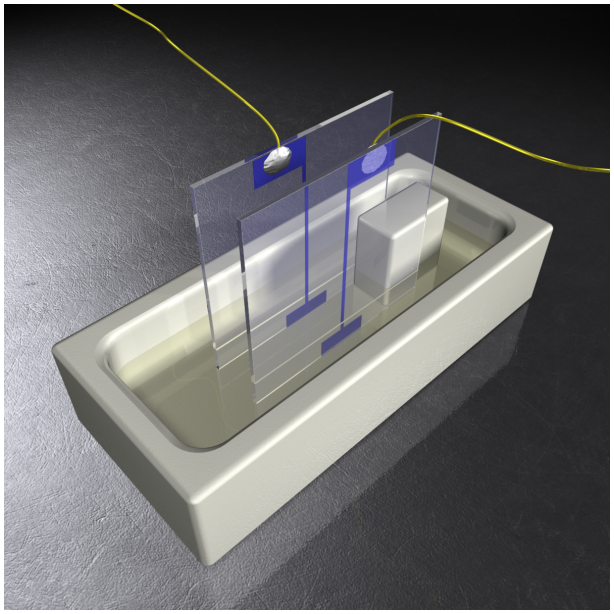


Figure 3.11.: Schematics of a parallel plate capacitor located in a Teflon boat. The second spacer on top of the plates is left out for better visibility of the setup. Reprinted with permission from [75]

In order to ensure exact parallel alignment spacers with thickness of 1 mm are attached on each side of the glass plate. The entire assembly is placed in a Teflon vessel, which serves as the reservoir for the CSPE, when still in the liquid state. With advancing solidification, the CSPEs undergo a mass loss of $\sim 90\,\%$. To account for it, the Teflon vessel is filled with the suited amount of liquid CSPE, to ensure that the final solid CSPE level matches the electrode height at the end of solidification process. The assembling of the parallel plate capacitors and the solidification processes are performed in an argon filled glove box.

3.3.6 Preparation of In-Plane Geometry FETs

The passive structures (electrodes) of the FETs are patterned from an ITO coated glass, using laser ablation. The FETs are prepared following the in-plane device geometry, as shown in the inset of Figure 3.12. The channel length is fixed to $50\,\mu$m.

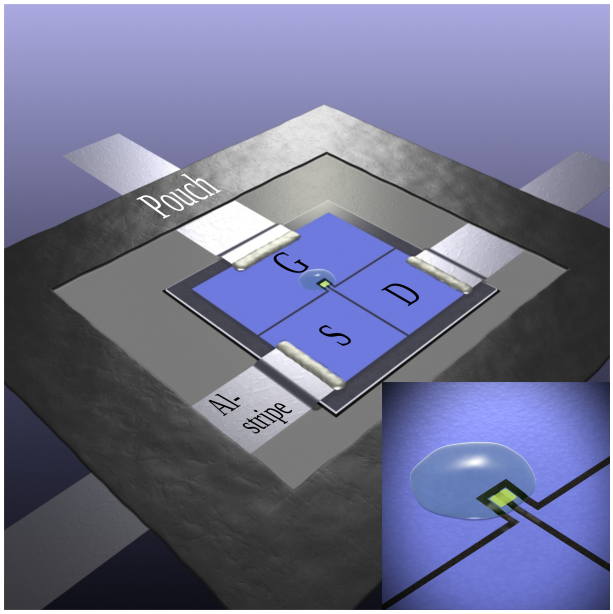


Figure 3.12.: Schematics of a fully processed in-plane FET. Electrodes are contacted by silver paste to aluminum stripes, which feed through the pouch protecting the device against external influences. The inset shows the channel in yellow with a CSPE layer covering the channel and a large portion of the gate electrode. Reprinted with permission from[75]

The structuring of the electrode is followed by a cleaning procedure using subsequently isopropanol (for analysis 99.5 %, Merck Millipore), acetone (for analysis 99.8 %, Merck Millipore) and ethanol (absolute 99.5 %, Merck Millipore). The In_2O_3 precursor and the CSPE are printed using the Dimatix 2831 desktop inkjet printer. The channel is prepared using the precursor solution described in 3.2.1. After printing the precursor, the substrate is placed on a hotplate at 100 °C for 10 min, followed by a heating step at 400 °C for 2 h in a box furnace (Nabertherm P330). To avoid contamination of the transistor channel, the CSPE is printed immediately after the annealing. A schematic of the channel region with printed CSPE can be seen in the inset of Figure 3.12. The electrolyte is printed to completely cover the channel and a large part of the gate electrode. Following the transistor preparation, aluminum stripes are connected to source, drain and gate electrodes. Then the device is sealed in a plastic pouch with Al-stripes leading out of the pouch for later contacting (schematically shown in Figure 3.12). To ensure good thermal contact for the measurement of the temperature dependent transistor characteristics, the substrate is glued to the inside of the pouch using a double sided electrically conducting carbon tape. Finally, the pouch is sealed by thermally interconnecting the plastic of the pouch with the aluminum contacts.

3.3.7 Preparation of Vertical Channel Geometry FETs

The vertical channel structures are prepared on Si/SiO_2 substrates with a 200 nm SiO_2 layer. The electrode structures consist of platinum (Pt, 99.99 %) and are structured by electron beam lithography. The Pt layer with a thickness of 100 nm is deposited in an ultrahigh vacuum chamber

using radio frequency sputtering. The pressure in the chamber is established by a constant flow of argon with a flow rate of 20 sccm to $3.3 \cdot 10^{-3}$ mbar. The power generator is set to a value of 20 W. A 5 μm thick layer of ITO was deposited as a sticking layer for better adhesion between SiO_2 and Pt. A schematic of the source and gate electrode is displayed in Figure 3.13(a).

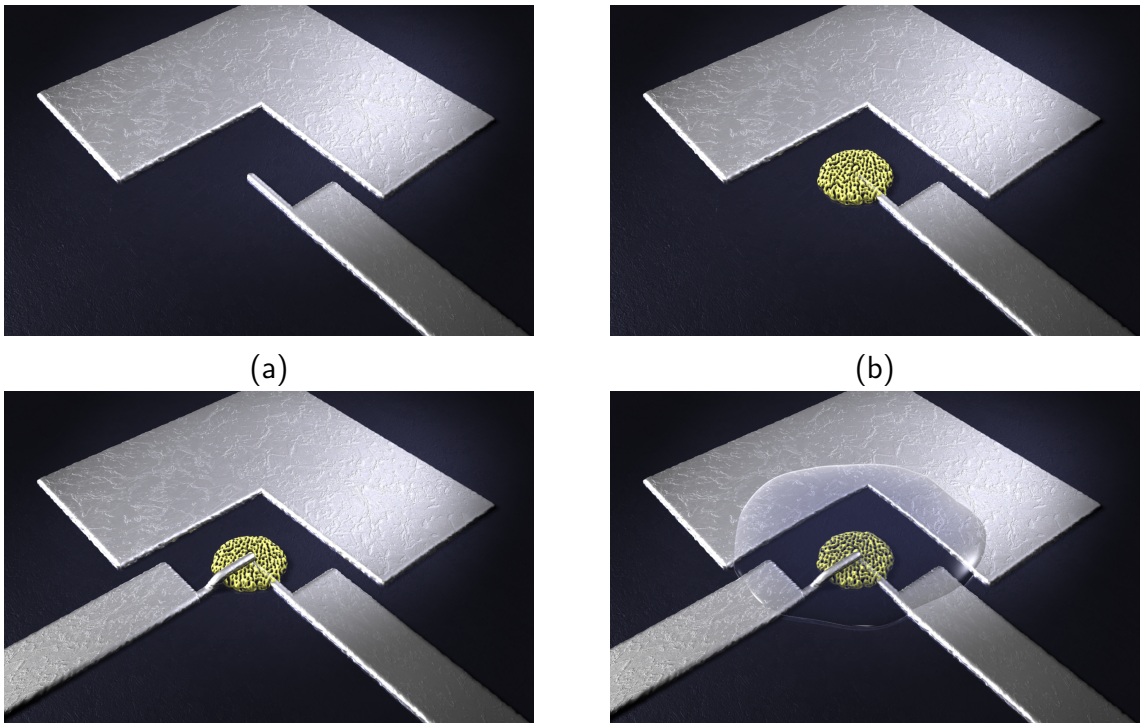


Figure 3.13.: Schematics of the deposition sequence on a 200 nm thick SiO_2 layer: (a) deposition of the Pt gate and source electrode, followed by (b) the dried SnO_2 precursor, which covers the tip of the source electrode, (c) the drain electrode and (d) the final coverage with CSPE.

In the next step a mild O_2 plasma is applied using a reactive ion etching chamber (Oxford Plasmalab 80 Plus, Oxford Instruments GmbH) for 30 seconds to clean the electrodes from remaining resist, which improves the surface properties of the substrate for better printing of the semiconductor. The precursor solution, introduced earlier in section 3.2.2, is printed carefully onto the source electrode. The source electrode has to be sufficiently covered by the precursor solution so that after drying no direct electrical contact with the drain electrode exists. This would otherwise lead to a short circuit and an unusable device. The precursor solution used for the channel preparation thereby ensures the porosity of the channel material. The functional principle will be explained in more detail in chapter 5. Figure 3.13(b) shows a schematic of the dried precursor material on top of the source electrode.

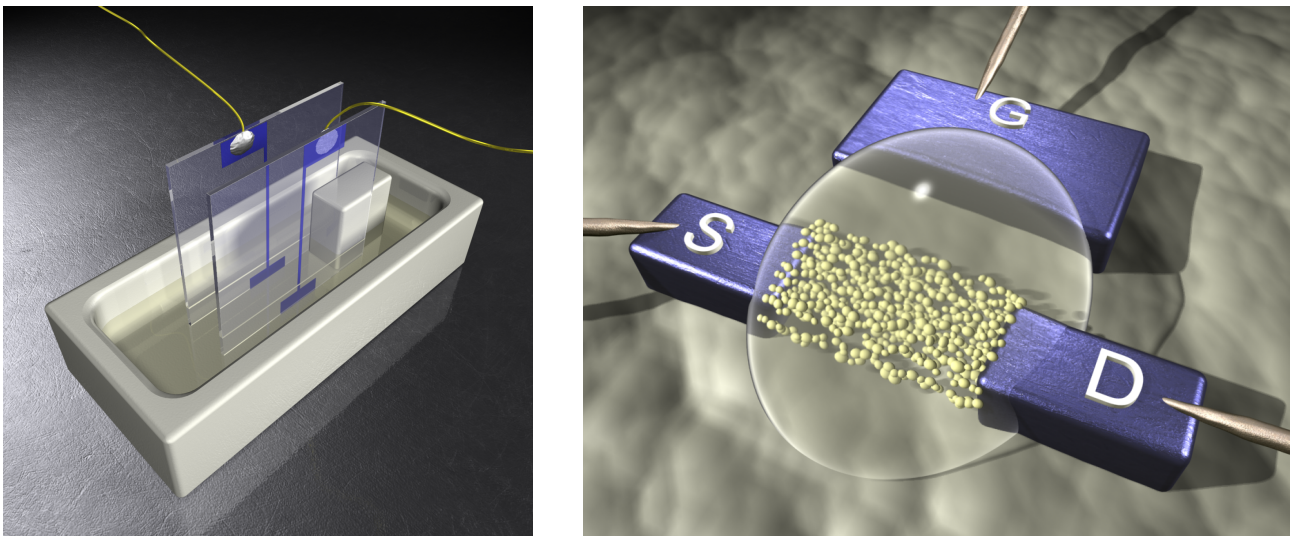
After printing the SnO_2 precursor, a second lithograph step is necessary to precisely apply the drain electrode on top of the channel area. Additionally the lithograph process is used to properly align source, channel and drain for the vertically aligned channel geometry. For the precise

positioning of the second electrode, marker structures are added during the first lithographic step to ease orientation on the substrate. Another platinum deposition step is performed and afterwards a lift-off is performed to finish the v-FET structure. Figure 3.13(c) shows a schematic of the stacked drive electrode geometry of the transistor together with a displaced gate electrode. After deposition of the drain electrode, the channel material undergoes a final heating step to 550 °C. Thereby the micelles are removed in a carefully optimized heating procedure with a ramp of 10 °C min^{-1} until reaching the maximum temperature of 550 °C. This temperature then was kept for 5 min followed by a cooling procedure under ambient condition down to room temperature. This heating step is not only necessary for the removal of the block-co-polymer but also for the conversion of $SnCl_4$ into SnO_2. Additionally, the heating is also beneficial for the interlayer contact between the platinum electrodes and the porous SnO_2 channel. Immediately after heating, the surface tensions of porous SnO_2 and the CSPE are not compatible and the infiltration of the porous structure does not work. Thus another O_2 plasma treatment is necessary to adjust the surface tension of the porous SnO_2, allowing the CSPE to penetrate the porous channels. Finally the CSPE is deposited via inkjet printing. The CSPE is thereby applied in a way that the channel area is completely covered to facilitate the infiltration into the channel region. In addition, a large area of the gate electrode compared to the channel area has to be covered to enable a proper channel formation in the porous semiconductor (see Figure 3.13(d)).

4 Temperature Dependence of Electrical Properties of Composite Solid Polymer Electrolytes

After introducing the theoretical background and the basic concept of the present thesis, the experimental results will be presented and discussed in detail. In order to find a suitable electrolyte for the application in FETs for daily use and with sufficient durability, several different electrolytes are tested for their chemical, mechanical and electrical properties. The aim is to find a CSPE, which shows high ionic conductivity and areal double layer capacitance over a large temperature range. The main focus of the present section is on the behavior of the CSPEs, especially at low temperatures. Understanding the temperature behavior of the CSPE then helps to design an FET with stable performance over a wide temperature range.

In this context three CSPEs are examined, which differ in the addition of liquid low melting point additives to improve the behavior at low temperatures.



(a) (b)

Figure 4.1.: Schematics of (a) an electrolyte filled parallel plate capacitor and (b) an electrolyte-gated nanoparticle channel field-effect transistor.

In the present thesis the additional demand of printability has to be fulfilled. Combining these requirements, a system consisting of a Lithium salt to ensure ionic conductivity, a polymer as a solidifying agent, a plasticizer to maintain a sufficient liquid phase in the final product and

a solvent to preserve printablility is designed. A plasticizer in this context describes a solvent with the special property to have a high boiling and low melting point and remain as a liquid component in the solidified final product. The final product after solidification is referred to as a composite solid polymer electrolyte, short "CSPE".

The chemical properties of three CSPEs, which use different plasticizers, are analyzed with respect to composition and change of their phase at low temperatures. Furthermore, the CSPEs are tested electrically by means of impedance spectroscopy in a CSPE filled parallel plate capacitor arrangement as shown in Figure 4.1(a). In this context a representative equivalent circuit is designed and used to determine the numbers of interest. Of main interest are thereby the changes in ionic conductivity σ_{el} and in the magnitude of the areal double layer capacitance C_{dl} with respect to temperature. As mentioned above, these figures influence the performance of electrolyte-gated field-effect transistors and thus are of particular interest. The goal is to find a suitable CSPE for an electrolyte-gated FET (EG-FET), which is stable in a large temperature range ($\sim$-30 °C to 50 °C) with favorably temperature independent, or at least predictable values of σ_{el} and C_{dl}. In the following study, the most suitable candidate is applied to field-effect transistors as a solid electrolyte gate dielectric. Such an FET is shown schematically in Figure 4.1(b). The characterization of the temperature dependence is essential for the later operation in logic circuits requiring a stable performance with constant values for the on-current and threshold voltage. In some preliminary experiments the suitability of such CSPEs for future application on flexible substrates is investigated. Mechanical stress tests in terms of rheology and tensile strength measurements are conducted and compared with literature data.

4.1 Chemical Properties of CSPEs

In the first section of this chapter the chemical properties of three different CSPEs are examined. Samples are prepared in petri dishes and dried under ambient conditions. From the weight loss the amount of ingredients after solidification is determined.

4.1.1 Material Composition of solid CSPEs

The materials for the electrolyte are chosen and tested at room temperature for their basic functionality. $LiClO_4$ salt is used because Li^+ is a very small ion, which can move easily in a solid or liquid electrolyte and thus is the best candidate to obtain a high ionic mobility. The plasticizers, namely PC, DEC and EMC, are used to retain a liquid component in the solidified CSPE to facilitate additionally the ion transport in the CSPE. Similar materials have shown their functionality as electrolytes in lithium ion batteries. In order to solidify the electrolyte, PVA with a low degree of polymerization is selected since earlier experiments have indicated that long PVA chains hinder the ion motion in the CSPEs. To guarantee also good printability, DMSO is added in sufficient

quantity to obtain a stable drop formation without clogging of the nozzles. The compositions of the three investigated CSPEs in liquid form (from now on referred to as CSPE(lq)) are listed in table 4.1.

Table 4.1.: Composition of as-prepared CSPEs(lq) before solidification.

CSPE	PVA [g]	$LiClO_4$ [g]	PC [g]	DEC [g]	EMC [g]	DMSO [g]
1	0.21	0.05	0.45	-	-	4.28
2	0.21	0.05	0.23	0.22	-	4.28
3	0.21	0.05	0.23	-	0.22	4.28

In order to determine the final amount of added solvent/plasticizer remaining in the CSPEs(sd) a controlled solidification is performed. CSPE(sd) is from now on refers to solidified CSPE. The CSPEs(lq) are spread in petri dishes to gain a high surface to volume ratio. The petri dishes are kept under ambient conditions in a fume hood and are weighed in certain intervals. After 28 days the weight reaches a constant value for at least three subsequent days and the CSPEs are considered solid. Based on thermogravimetric measurements combined with mass spectroscopy experiments conducted by Nasr et al. [59] it can be assumed, that the solid ingredients like $LiClO_4$ and PVA do not evaporate and therefore the remaining quantity of solvent/plasticizers can be determined.

Table 4.2.: Composition of the three investigated dried CSPEs.

CSPE	PVA [g]	$LiClO_4$ [g]	DMSO, PC, DEC and EMC [g]
1	0.21	0.05	0.15
2	0.21	0.05	0.18
3	0.21	0.05	0.13

Table 4.2 shows the final composition of the CSPEs(sd). The experiments prove that a considerable amount of solvent and added plasticizer(s) remain in the CSPEs(sd). The exact composition of the liquid components cannot be determined with this experiment but a liquid phase is present without any doubt.

4.1.2 Phase Transitions of CSPEs

After knowing that all three CSPEs(sd) contain a liquid phase at room temperature, it is interesting to know if there will be a phase transformation of this liquid phase to a solid phase especially

at low temperature. Such a change in phase would influence the performance of a field-effect transistor, especially due to the expected change of the ionic conductivity of the CSPEs(sd). The experiment is conducted exemplarily on CSPE-1, which has the simplest composition of the investigated CSPEs. Taking a look at the freezing temperatures of the solvent and the plasticizer(s) (see appendix, table F.1), PC has a freezing temperature of -48.8 °C and DMSO freezes at 18 °C. In a complex mixture of different materials the freezing points of the individual components usually do not show up. The freezing point of an ionic conductor thereby influences the viscosity, and the viscosity on the other hand influences the ionic conductivity. Therefore, it is important to understand the phase transformations of such a mixture. In order to determine the phase transformations differential scanning calorimetric (DSC) measurements are conducted on CSPE-1 before and after solidification in a temperature range between -100 °C and +25 °C. For the DSC measurements samples are prepared in an aluminum boat and solidified in ambient conditions. Figure 4.2(a) shows the differential scanning calorimetry data of the liquid sample and Figure 4.2(b) those of the solidified sample. The exothermic feature at ∼-25 °C during cooling of the liquid sample can be interpreted as a phase transition from the liquid to the crystalline state. The phase transition from the crystalline to the liquid phase at ∼0 °C during subsequent heating is of endothermic nature. The freezing temperature is shifted towards lower temperatures compared to the melting point. This supercooling happens because of a lack of crystalline nuclei, which act as nucleation sites for the crystallization. Without nucleation sites the liquid has to perform a spontaneous crystallization, which can occur, depending on the cooling rate, several tens of degrees below the actual freezing temperature.

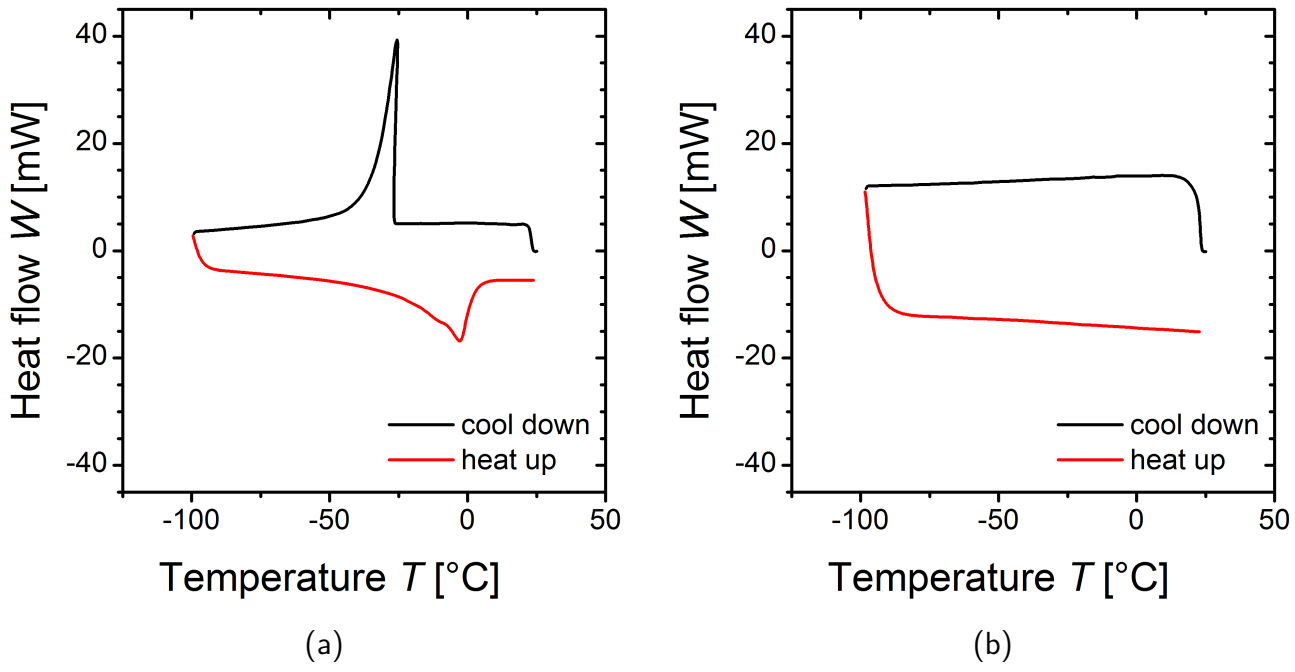


Figure 4.2.: Differential scanning calorimetry measurements of (a) liquid and (b) solidified CSPE-1 samples. The scanning rate was 10 °C/min.

During warm up this effect does not occur because melting happens right at the actual melting temperature. The actual freezing point of the compound is $\sim 0\,°C$ which does not correspond to the freezing temperature of the pure solvents, as anticipated before. The DSC data of the solidified sample does not show any feature of a phase transformation in the investigated temperature range. This behavior implies that for the solid phase no phase transformation takes place in a temperature range down to -100 °C being particularly beneficial for the performance of the CSPE(sd) and of an electrolyte-gated field-effect transistor at low temperatures.

4.2 Electrical Properties of Composite Solid Polymer Electrolytes

The lack of phase transitions is encouraging for the use of the CSPEs(sd) as a dielectric suitable for an all solid state transistor. In order to determine the ultimate performance and to understand the performance of the transistor the electrical properties of the CSPE(sd) need to be investigated. This is done in a parallel plate capacitor arrangement (see section 3.3.5), since the geometrical parameters such as electrode sizes and distance between the electrodes are easy to control. The method of choice is temperature dependent impedance spectroscopy to determine ionic conductivity σ_{el} and areal double layer capacitance C_{dl}. The measurements are conducted in a temperature range between -45 °C and 45 °C where everyday electronics are supposed to operate properly. The measurements are conducted to examine how future transistors will be influenced by the dielectric when operated at those temperatures. The impedance spectroscopy allows both, σ_{el} and C_{dl}, to be investigated at once and their values can be extracted independently. Furthermore, impedance spectroscopy is a non-destructive technique, which allows performing many measurements with the same sample avoiding variations due to differences in sample preparation.

4.2.1 Capacitive CSPE Based Devices

In the following section, the results from impedance spectroscopy of three different CSPEs(sd) are presented and discussed. The development of an equivalent circuit is described in detail and validated during the solidification process of the CSPEs. The temperature dependent behavior of σ_{el} and C_{dl} is extracted and models are discussed to describe the observed behavior. In a first step the final geometry of the parallel plate capacitor has to be found. After several trails with different electrode sizes and electrode gaps the final geometry of the parallel plate capacitor is fixed to 2 mm × 1 mm and a gap of 1 mm, respectively. With this geometry all the following measurements are conducted.

Equivalent Circuit Determination

To identify the components of an equivalent circuit representing the measuring setup, a detailed analysis of the setup and the physical processes occurring in the CSPEs is performed.

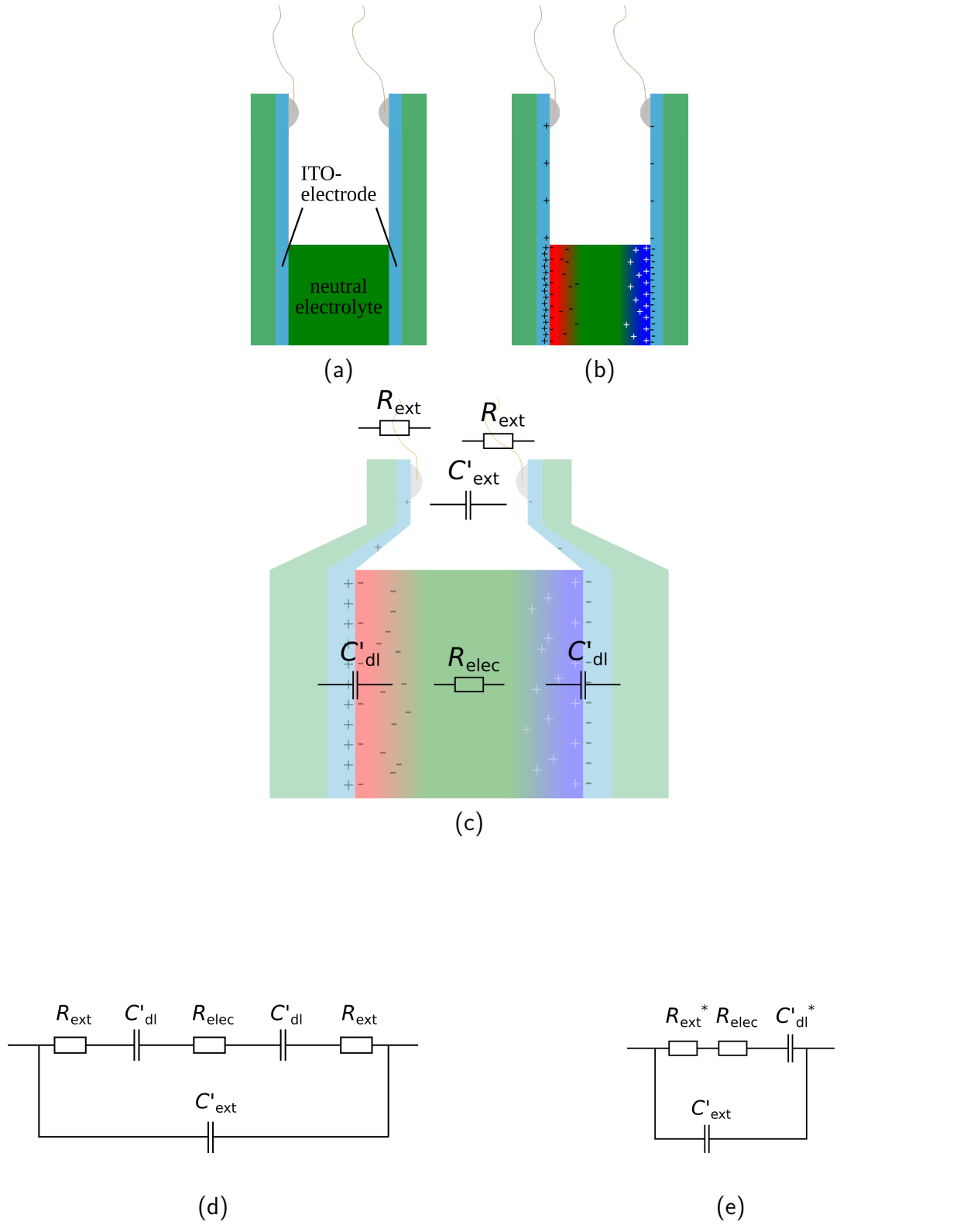


Figure 4.3.: Graphic illustration of the determination of the equivalent circuit: (a) schematic of an uncharged CSPE filled parallel plate capacitor, (b) a charged capacitor with charge separation and formation of the electrical double layers, (c) presentation of the electric components correlated to the respective components of the measuring setup, (d) an equivalent electrical circuit as extracted from the measuring setup and assembled in logic order and (e) a reduced condensed equivalent electrical circuit equal to the one shown in (d).

Figure 4.3(a) shows a schematic of the prepared parallel plate capacitor (see section 3.3.5) without an applied voltage between the ITO electrodes. Above the part covered by CSPE the ITO layer is reduced in width and forms a lead to the contact pads at the top of the glass plate (see Figure 4.1(a)). At the contact pads gold wires are connected using silver based epoxy glue for connecting the setup to the impedance spectrometer. Under an applied voltage, as seen in Figure 4.3(b), the ions in the CSPE are separated and form an electrical double layer as discussed in section 2.3.1. As described by Otto Stern this charge separation causes the formation of an electrical double layer close to the charged interfaces composed of the Helmholtz double layer and the Gouy-Chapman diffuse double layer. The bulk of the CSPE in between the two double layers is electrically neutral, still containing positive and negative ions compensating each other. Since all discussed circuit components contribute to the measurement signal they have to be included in the equivalent circuit. In Figure 4.3(c) the correlation between the physical processes occurring in the measuring setup with electrical circuit elements are proposed. The leads between the impedance spectrometer and the ITO electrodes of the CSPE filled capacitor are represented by the resistors R_{ext}. These resistors also include the resistance of the ITO electrodes. The capacitance created by those leads and the ITO electrodes is represented by the capacitor C'_{ext}. The electrical double layers are represented by two capacitors with the capacitance C'_{dl} at the interface between ITO electrode and CSPE. The bulk CSPE, even though no net charge is present, contains ions from the dissolved salt and is represented by the resistor R_{el}.

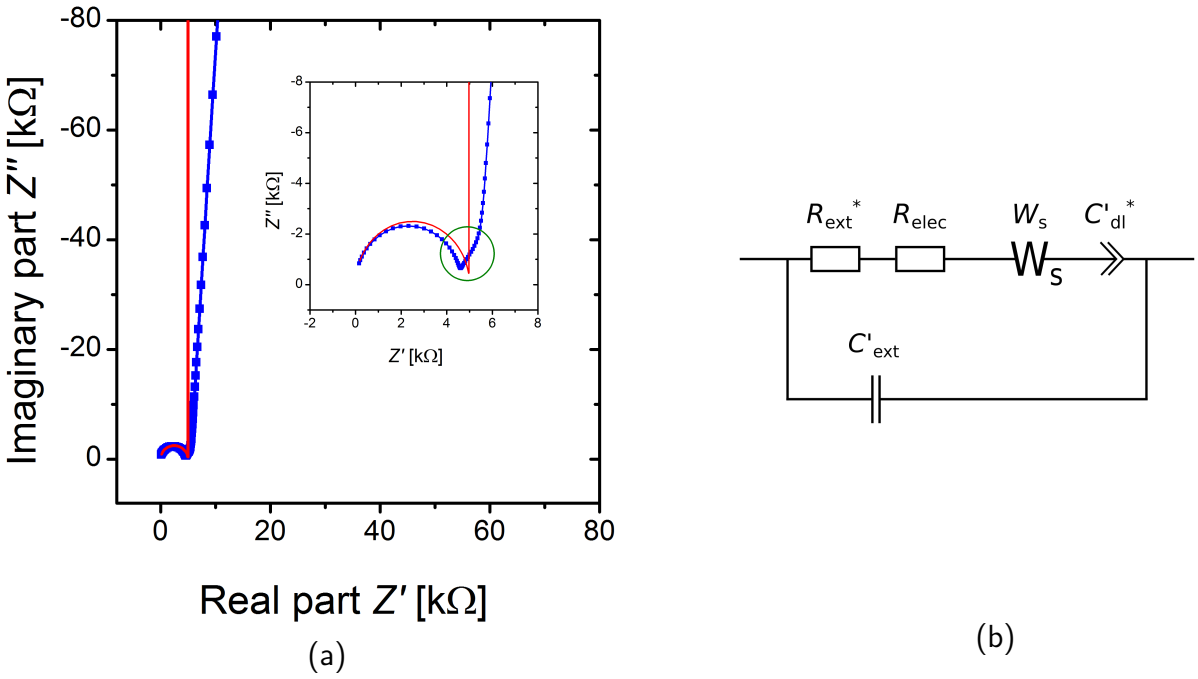


Figure 4.4.: (a) Nyquist plot of a CSPE-1 filled parallel plate capacitor measured at room temperature (blue) and the fitted curve using the equivalent circuit from Figure 4.3(e) and (b) the modified equivalent circuit.

Putting together all the components in the logical order one ends up with the equivalent circuit shown in Figure 4.3(d). Since the setup is completely symmetric, the equivalent circuit can be simplified and condensed to the circuit shown in Figure 4.3(e) with ${R_{\text{ext}}}^* = 2\,R_{\text{ext}}$ and ${C'_{\text{dl}}}^* = 1/2\,C'_{\text{dl}}$. With this equivalent circuit the data can be generally fitted, but not every feature of the measured data can be represented accurately (see Figure 4.4(a)). To improve the fit of the measured data, two adjustments have been made. First, the tilt of the low frequency section in the measured data is taken into account by a constant phase element to replace the capacitor C_{dl}. A constant phase element is taking the diffusive part of the electrical double layer, i.e., the Gouy-Chapman layer into account. This adjustment is meaningful and allows to fit the low frequency region of the Nyquist plot more accurately. The second adjustment is to introduce an element, which can explain the $\sim 45\,^\circ$ section, which is marked with a green circle in Figure 4.4(a). In literature such a phenomenon has been reported when investigating polymer electrolytes and was described with a Warburg element in series to the constant phase element [76]. Another way to fit the data in this specific frequency region is an additional RC circuit in series to the constant phase element. At this point, a discussion about which way to describe it as well as about the origin of such a behavior would be speculative and is not advisable, because the physical and chemical background for a proper explanation is not given. Anyhow, for the measurements conducted during this thesis, which are all DC measurements, this component has no influence. In the impedance picture, the closest to DC is in the low frequency region. In this region the constant phase element is the predominate component of the equivalent circuit, regardless which component is used to describe the $\sim 45\,^\circ$ section. With a Warburg element as well as with the RC circuit in series with the constant phase element, the resulting double layer capacitance only changes by $<1\,\%$. The equivalent circuit used for further fitting contains the Warburg element. With the modified equivalent circuit, a function can be calculated to fit the measured data satisfactorily. The impedances of the utilized electrical elements can be seen in the following equations:

Resistor: $$Z_R = R \tag{4.1}$$

Capacitor: $$Z_C = \frac{1}{i\omega C} \tag{4.2}$$

Constant Phase Element: $$Z_{CPE} = \frac{1}{(i\,\omega)^\alpha\, C} \tag{4.3}$$

Warburg short: $$Z_{W_\text{s}} = W_\text{R}\,\frac{\tanh[(i\,\omega\,W_\text{T})^{W_\text{P}}]}{(i\,\omega\,W_\text{T})^{W_\text{P}}} \tag{4.4}$$

Using the classic addition theorems of the respective components the equivalent circuit can be expressed using the following term:

$$Z = \frac{\left(R^*_{\mathrm{ext}} + R_{\mathrm{el}} + \frac{W_{\mathrm{R}}.\tanh[(i\omega W_{\mathrm{T}})^{W_{\mathrm{P}}}]}{(i\omega W_{\mathrm{T}})^{W_{\mathrm{P}}}} - \frac{1}{(i\omega)^{\alpha} C'^*_{\mathrm{dl}}} \right) \cdot \frac{-1}{i\omega C'_{\mathrm{ext}}}}{R^*_{\mathrm{ext}} + R_{\mathrm{el}} + \frac{W_{\mathrm{R}}.\tanh[(i\omega W_{\mathrm{T}})^{W_{\mathrm{P}}}]}{(i\omega W_{\mathrm{T}})^{W_{\mathrm{P}}}} - \frac{1}{(i\omega)^{\alpha} C'^*_{\mathrm{dl}}} - \frac{1}{i\omega C'_{\mathrm{ext}}}} \tag{4.5}$$

This equation can be separated into a real and an imaginary part and can be used to fit the measured data of the Nyquist plot. The fitting is necessary to determine the absolute value of each component of the equivalent circuit. The quality of the fit is an indicator how well the values of the different components represent the behavior of the measured setup. In the following all fits of the impedance spectroscopy data are performed using the same electrical equivalent circuit shown in Figure 4.4(b).

To confirm the correctness of the equivalent circuit one representative CSPE (CSPE-1(lq)) is measured during the solidification process. During that process certain quantities are changing: e.g., the electrolyte conductivity has to decrease during the solidification process. This behavior is expected, because the ionic conductivity is dependent on the ion mobility of the dissolved salt in the CSPE. The ionic conductivity σ_{el} can be extracted from R_{el} using the basic relation:

$$\sigma_{\mathrm{elec}} = \frac{1}{R_{\mathrm{elec}}} \frac{A}{d} \tag{4.6}$$

where d is the electrode distance and A is the electrode area. Figure 4.5(a) displays the extracted ionic conductivity with solidification time. The increasing viscosity during the ongoing solidification process (see below in section 4.3.1) reduces the ionic mobility and therewith the ionic conductivity. The constant value of σ_{el} after 8 days indicates that the CSPE(sd) has reached a stable state. In general the temperature dependence of the ionic conductivity reflects the expected behavior. At this point it should be mentioned, that such a long period is owed to the large amount ($\sim$2 ml) of CSPE(lq) necessary to fill the parallel plate capacitor entirely. In a printed device the quantities are orders of magnitude smaller and the solidification takes only minutes. The areal double layer capacitance C_{dl} on the other hand does not change during solidification as can be seen from Figure 4.5(b). This indicates that the magnitude of the areal capacitance at the CSPE/ITO interface is not influenced by the solidification process. It shows that the remaining plasticizer/solvent mixture is not preventing the ions in the bulk of the CSPE-1(sd) to reach and approach the interfaces.

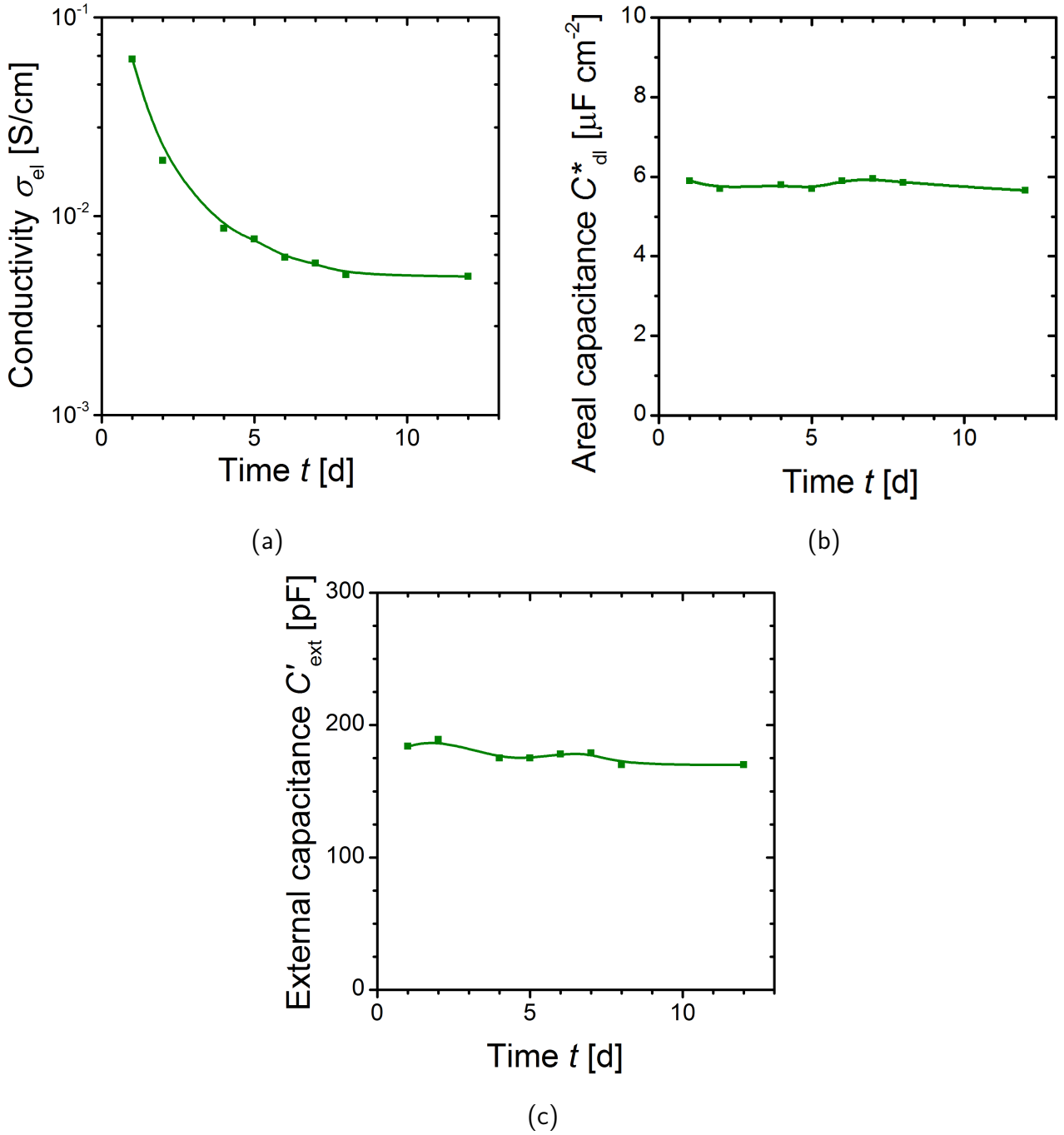


Figure 4.5.: Development of electrical parameters of the CSPE-1(lq) filled parallel plate capacitor with solidification time: (a) electrolyte conductivity σ_{el}, (b) areal double layer capacitance C_{dl} and (c) the external capacitance C'_{ext}.

Figure 4.5(c) shows the behavior of the external capacitance obtained from the impedance spectroscopic fits. A constant value of the capacitance C'_{ext} during solidification is obtained. This result is meaningful since the affected components like the external lead capacitance and the geometry of the parallel plate capacitor are not changing in the solidification process. This result can be considered as an additional indicator that the equivalent circuit is chosen in a meaningful way and represents the measured setup. After having laid the basis for a meaningful equivalent

circuit of the measuring setup, Bode plots of the CSPE-1(sd) filled parallel plate capacitor are measured and displayed in Figure 4.6. The measurement is performed at room temperature and covers the frequency range from 1 MHz to 1 Hz. Figure 4.6(a) shows the course of the phase angle φ with respect to frequency. It indicates at low frequencies up to about 90 Hz a phase angle of almost 90 °, which resembles a capacitive behavior. From 90 Hz to about 10^5 Hz a phase angle of 0 ° represents a resistive behavior and at higher frequencies a capacitive behavior is dominant, again. In the double logarithmic plot of the absolute impedance $|Z|$ with respect to frequency (see Figure 4.6(b)) the three frequency regions as described before can also be recognized. Starting from low frequencies a linear decrease is observed followed by a plateau and again followed by a linear decrease. This confirms, that both Bode plots contain the information, in which frequency region which component of the equivalent circuit is dominant.

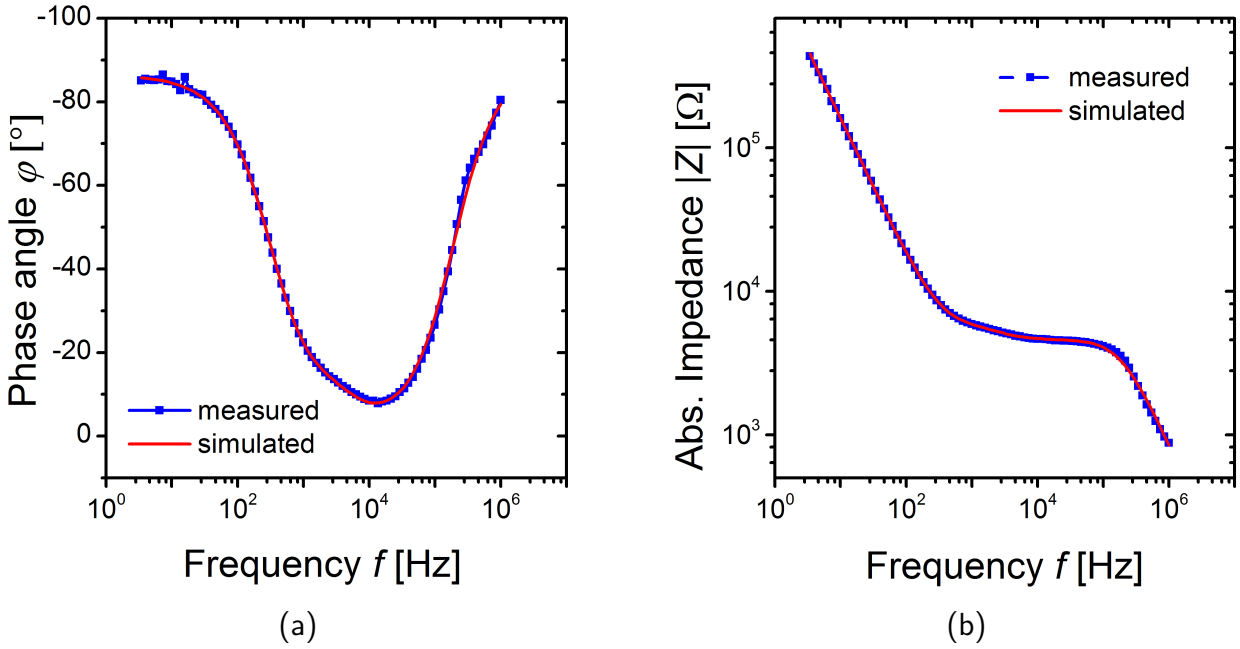


Figure 4.6.: Bode plots of an impedance spectroscopy measurement performed with the parallel plate capacitor filled with CSPE-1(sd): (a) the frequency dependence of the phase angle φ and (b) the frequency dependence of $|Z|$.

Figure 4.7 shows the Nyquist plot related to the Bode plots from Figure 4.6. For $Z' \lesssim 5\,\mathrm{k\Omega}$ or $f = 5\,\mathrm{kHz}$, respectively, a semicircle is visible, which is shown in a zoomed graph in the inset of Figure 4.7. For larger values of Z', or lower frequencies, two linear regimes with different slopes can be distinguished. The Nyquist plot provides information about the arrangement of the respective components in the equivalent circuit and is used to fit the values of its components.

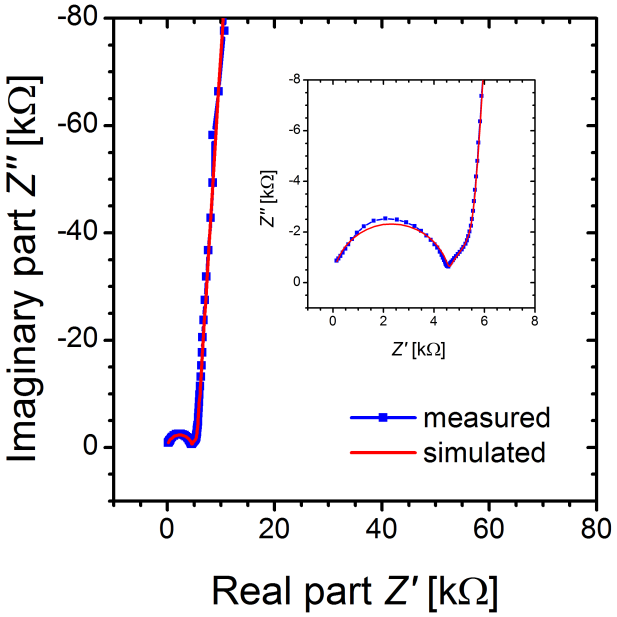


Figure 4.7.: Nyquist plot related to the Bode plots of Figure 4.6 obtained from a CSPE-1(sd) filled parallel plate capacitor. The inset shows an enlarged view of the high frequency part of the Nyquist plot.

Before measuring the temperature dependence of the characteristic quantities such as the ionic conductivity σ_{el} and the areal double layer capacitance C_{dl} of the CSPEs(sd) the different CSPEs(sd) are compared at room temperature. The obtained Nyquist plots, which compare the high frequency regime of all three CSPEs(sd), are displayed in Figure 4.8.

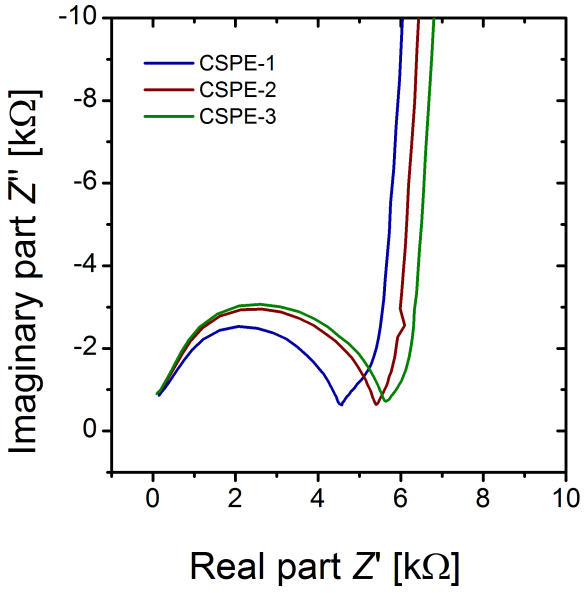


Figure 4.8.: High frequency section of the Nyquist plots of parallel plate capacitors filled with CSPE-1(sd), -2(sd) and -3(sd).

The smaller semicircle for CSPE-1(sd) indicates a higher conductivity compared to CSPE-2(sd) and CSPE-3(sd). This result can be verified by fitting the respective Nyquist plots to the equivalent electrical circuit. The results for the ionic conductivity σ_{el} are $5.4{\cdot}10^{-3}$S cm^{-1}, $3.3{\cdot}10^{-3}$S cm^{-1} and $2.9{\cdot}10^{-3}$S cm^{-1} for CSPE-1(sd), CSPE-2(sd) and CSPE-3(sd), respectively. From the same fits also the results for the areal double layer capacitances C_{dl} are determined. They amount to 6.0 μF cm^{-2}, 5.3 μF cm^{-2} and 5.5 μF cm^{-2}, for the same CSPEs. This indicates a superior behavior of CSPE-1(sd) compared to the other two composite solid polymer electrolytes in terms of σ_{el}, which determines the switching speed of the device and C_{dl}, which determines also the switching speed and the utilized gate voltage to form the conducting channel. In both cases higher values of σ_{el} and C_{dl} are beneficial.

Temperature Dependence of CSPEs(sd)

In a next step the temperature dependencies of the conductivity and the areal double layer capacitance of the three CSPEs(sd) are determined. The temperature dependence of σ_{el} and C_{dl} are important properties, since they determine the stability of electric circuits when such EG-FETs are integrated and used under ambient conditions. The experiments are performed in the same manner as in the previous section. In order to introduce the temperature variation, the measurements are conducted on a temperature controllable heating/cooling stage. The temperature is calibrated in a test setup utilizing the same devices, however, with a thermocouple in between the glass plates. The measurements are conducted in an application relevant temperature range between -45 °C and 45 °C.

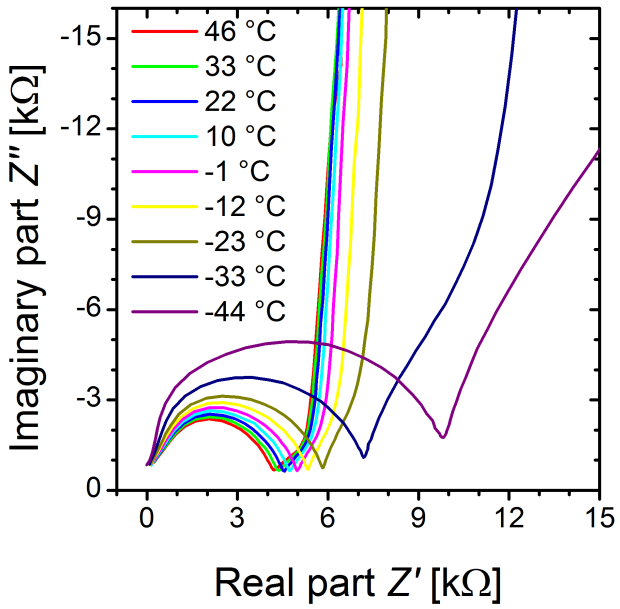


Figure 4.9.: Nyquist plots of a CSPE-1(sd) filled parallel plate capacitor measured at different temperatures.

Figure 4.9 shows the Nyquist plots of a CSPE-1(sd) filled parallel plate capacitor for high frequencies measured at temperatures between -45 °C and 45 °C. At every temperature a thermalization step of 20 minutes is allowed to guarantee thermal equilibrium. The observed increase of the diameter of the semicircle with decreasing temperature is synonymous for an increasing electrolyte resistance or equivalently a decreasing ionic conductivity. Since in the high frequency region R_{ext}, R_{el} and C'_{ext} are the predominant components the increasing diameter of the semicircle is representing an increase of R_{el}, which represents the bulk resistance of the CSPEs(sd), because R_{ext} and C'_{ext} are constant during the temperature sweep. The section after the semicircle towards lower frequencies is described by the Warburg element as stated earlier. Since this part does not influence the outcome of the following analysis it will not further be discussed. In the low frequency region, the constant phase element is the predominant component. Like in the last section 4.2.1 the curve resulting from eq. (4.5) is fitted to the measured data displayed in the Nyquist plot. This fitting routine is conducted for the data at different temperatures and the values for the ionic conductivity and the areal double layer capacitance are extracted as a function of temperature. From these values the two most relevant parameters, namely σ_{el} and C_{dl} are determined where the ionic conductivity of the electrolyte is calculated from eq. (4.6) and the areal double layer capacitance is calculated from ${C'_{\mathrm{dl}}}^*$ using

$$C'_{\mathrm{dl}} = \frac{C'^*_{\mathrm{dl}}}{A} \tag{4.7}$$

with A the electrode area. Figure 4.10 shows σ_{el} and C_{dl} as functions of temperature. An increasing ionic conductivity with temperature is expected, since it depends on the movement of ions in the CSPEs(sd) and an increased temperature reduces the viscosity of the CSPEs(sd). Since no simple Arrhenius dependence was applicable for the temperature dependence of the ionic conductivity, another model developed by Vogel, Tamman and Fulcher (VTF model) [77–79] is used. This model was also shown to be applicable to PC containing electrolytes behaving like glass forming substances [80]. Using this model the conductivity can be described as follows:

$$\sigma = \sigma_0 \exp\left(\frac{-B}{T - T_0}\right) \tag{4.8}$$

where σ_0 and B describing the conductivity at T_0 and the activation energy of the material, respectively. The temperature T_0 is thereby related to the glass transition temperature and is

usually found ∼50 °C below T_g resulting in $T_g = T_0 + 50\,°C$ [80]. The equation is fitted to the measured data and yield the glass transition temperatures for the three materials as:

$$\text{CSPE-1(sd)}: T_g \approx -130\,°C \tag{4.9}$$

$$\text{CSPE-2(sd)}: T_g \approx -56\,°C \tag{4.10}$$

$$\text{CSPE-3(sd)}: T_g \approx -41\,°C. \tag{4.11}$$

The glass transition temperature of CSPE-1(sd) is determined well below -100 °C, which is in agreement with DSC measurements (see Figure 4.2(b)). For the other CSPEs(sd) T_g also seems to be below the measured temperature range, which can be deduced from the smooth shape of the experimentally determined electrolyte conductivity and fitted data using the VTF model as displayed in Figure 4.10(a). The highest conductivity can be assigned to CSPE-1(sd) for the entire temperature range. This makes CSPE-1(sd) an even stronger candidate for the application in EG-FETs. However, the conductivity of the electrolyte is not exclusively determining the suitability of the candidate. A second factor is the areal double layer capacitance. Figure 4.10(b) shows the development of the areal double layer capacitance of the three CSPEs(sd). Despite the offset in y-direction, the three CSPEs(sd) show the same principle dependence on temperature.

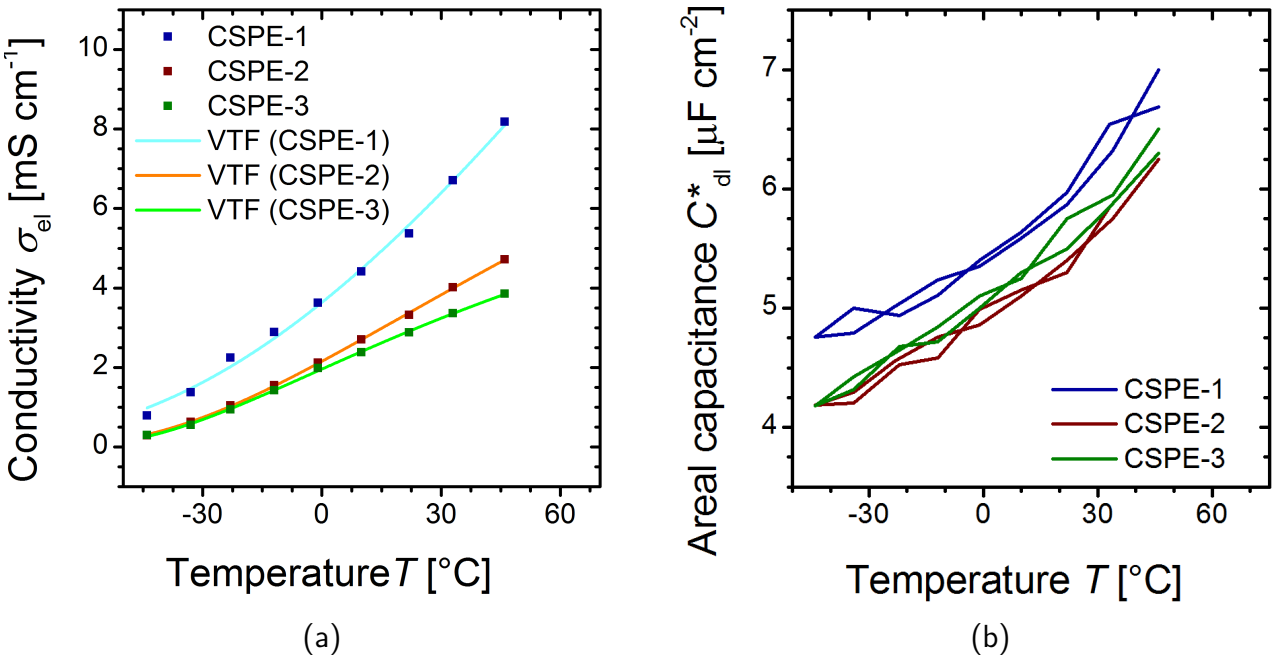


Figure 4.10.: (a) Electrolyte conductivity and (b) areal double layer capacitance (squares) as a function of temperature as obtained from impedance spectroscopic analysis of the three utilized CSPEs(sd). The continuous lines in (a) resemble the simulated curves using the VTF model [80].

The measured values of CSPE-2(sd) and -3(sd) do not vary a lot but CSPE-1(sd) shows the highest areal capacitance C_{dl}. The increase of C_{dl}, in general, is somewhat surprising, since the opposite behavior is suggested by theory. Following the law of Stokes for the radius of an ion including its solvation shell the radius is supposed to increase with temperature. The hydrodynamic radius R_{hyd} is calculated from

$$R_{hyd} = \frac{k_B T}{6\pi\eta D} \tag{4.12}$$

with k_{B} the Boltzmann constant, T the absolute temperature, η the viscosity and D the diffusion coefficient. According to this equation the radius of the solvation shell grows with rising temperature. Since the areal capacitance C_{dl} is formed between the ions in the CSPE(sd) and the compensation charges in the semiconductor one would expect a reduced areal capacitance with growing R_{hyd}. The experimental values of the areal capacitance show, however, a potential growth of the kind

$$C_{\mathrm{dl}} \propto 1/R_{\mathrm{hyd}} \propto T^{\gamma} \tag{4.13}$$

with $1 < \gamma < 2$. This dependency cannot be explained with the change of the solvation shell radius. Other possible explanations for such a behavior can be an increased number of available ions for the double layer formation at higher temperatures.

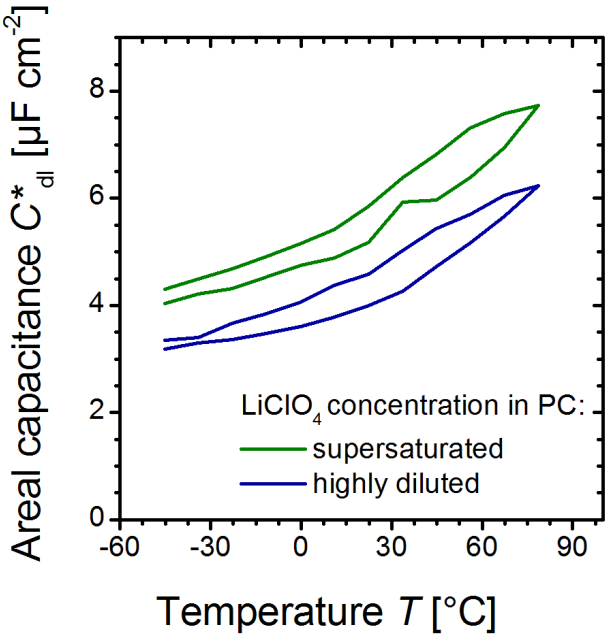


Figure 4.11.: Areal double layer capacitance as a function of temperature extracted from impedance spectroscopy data for two different electrolyte solutions. Green represents a supersaturated solution of $LiClO_4$ in PC while blue represents a highly diluted solution.

If the electrolyte salt crystallizes during the solidification process and evaporation of the solvent/-plasticizer due to supersaturation, the increased solubility with elevated temperature would make

more ions available. This could explain the positive behavior of C_{dl} with temperature. Two experiments have been performed to check this hypothesis, namely X-ray diffraction to check for crystalline $LiClO_4$ in the dried material and impedance spectroscopy of a supersaturated and a highly diluted $LiClO_4$ in PC solution. The XRD measurements did not show any specific reflexes correlated to crystalline $LiClO_4$. This does not mean necessarily that no crystals have been formed. The size and density of the $LiClO_4$ crystals could simply be too small to be detected. The impedance spectroscopy analysis of the supersaturated and the highly diluted solutions show the same increase of the areal capacitance C_{dl} with temperature for both solutions as the CSPEs(sd)(see Figure 4.11). From the combination of these two experiments it is conducted, that the assumption made above, i.e., the crystallization of $LiClO_4$ during the solidification of the CSPE(lq), cannot explain the observed behavior. A further explanation could be the reduction of the bond strength between the ions and their solvation shell with temperature. Whereas in a neutral CSPE(sd) the ions are neutralized by the solvation shell, the situation changes in an electrical double layer. In this case the neutralization is done partly by charges of the electrodes. A weaker bonding of the solvation shell with temperature could ease the approach of the ions to the electrode and reduce the average distance to the surface of the electrode. In this way the increase of the areal capacitance could be explained.

4.2.2 Electrolyte-Gated Field-Effect Transistors

After analyzing the CSPEs(sd) in terms of impedance spectroscopy in a parallel plate capacitor, CSPE-1(sd) is considered the most suitable candidate for using in the field-effect transistors. The successful applicability of CSPEs to such devices could be very relevant for future developments in printed circuits and logics.

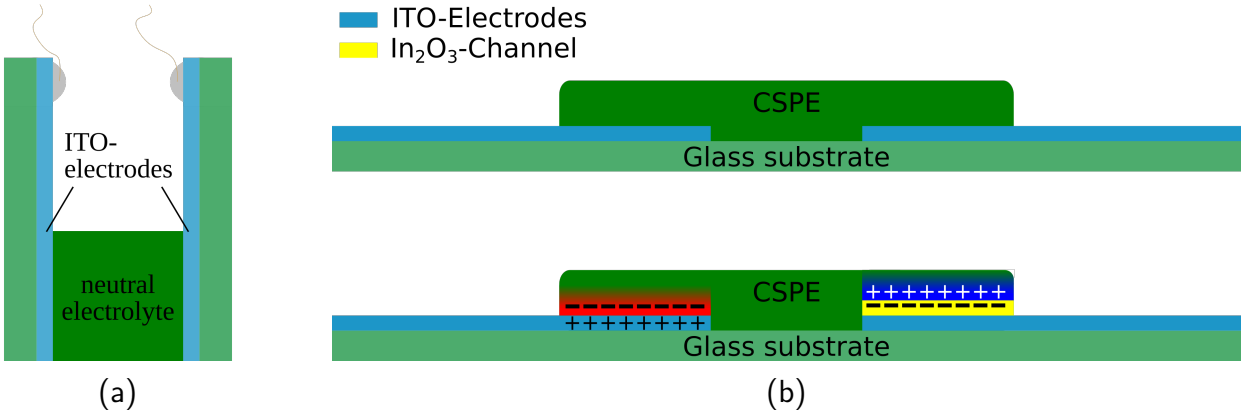


Figure 4.12.: Schematic of the function of an EG-FET: (a) a neutral parallel plate capacitor, (b) an uncharged in-plane capacitor (top) and a charged in-plane capacitor with In_2O_3 channel (bottom).

To investigate the properties of CSPE-1, a well established device geometry was chosen, whose performance has been investigated at RT intensively [2, 20–23]. Figure 4.12(a) shows a parallel plate capacitor as described above for the characterization of CSPEs using impedance spectroscopy. After back folding the capacitor plates, an in-plane capacitor geometry is formed as seen in Figure 4.12(b) (top).

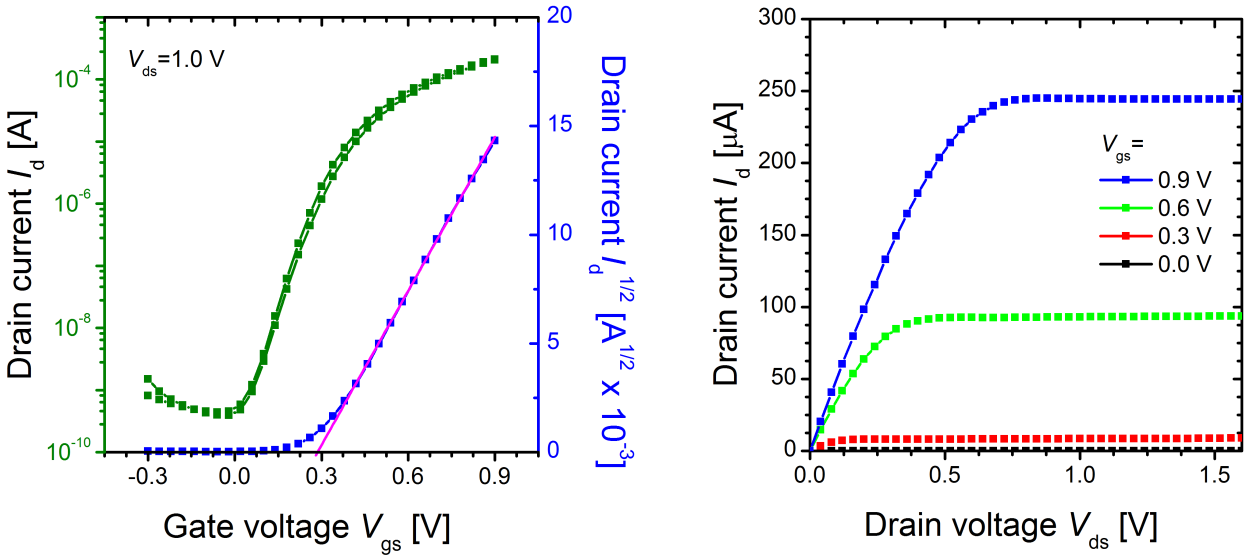


Figure 4.13.: Transfer (a) and output (b) curves of an in-plane EG-FET measured at room temperature.

If an In_2O_3 channel is added on top of the right ITO electrode and a positive voltage is applied to the left ITO electrode of the in-plane capacitor the system works just like the parallel plate capacitor due to the formation of an electrical double layer. The In_2O_3 counter electrode will be charged by the field-effect. A schematic side view of an in-plane FET is seen in Figure 4.12(b) (bottom). Such a field-effect transistors with ITO passive structures, In_2O_3 channel on top of a glass substrate have proven to work reliable in ambient conditions. An identical FET was measured and characterized in the temperature range between -35 °C and 60 °C. The output and transfer curves as seen in Figure 4.13 are analyzed as described in section 3.1.8 for each individual temperature. Off-current, on/off-current ratio, subthreshold swing, threshold voltage, field-effect mobility and on-current are extracted from the respective transfer curves. In the following sections, a red circle marks the position(s), where the respective data is extracted from. The respective extracted values are plotted as a function of temperature in a separate graph. The trend is analyzed and compared to theoretical predictions whenever possible. At the end of the chapter a brief analysis of the switching speed related to the time constants as derived from the experiments is given.

Off-Current

The off-current describes the leakage current between source and drain in the off state of the FET. A low off-current is important to ensure low static power consumption.

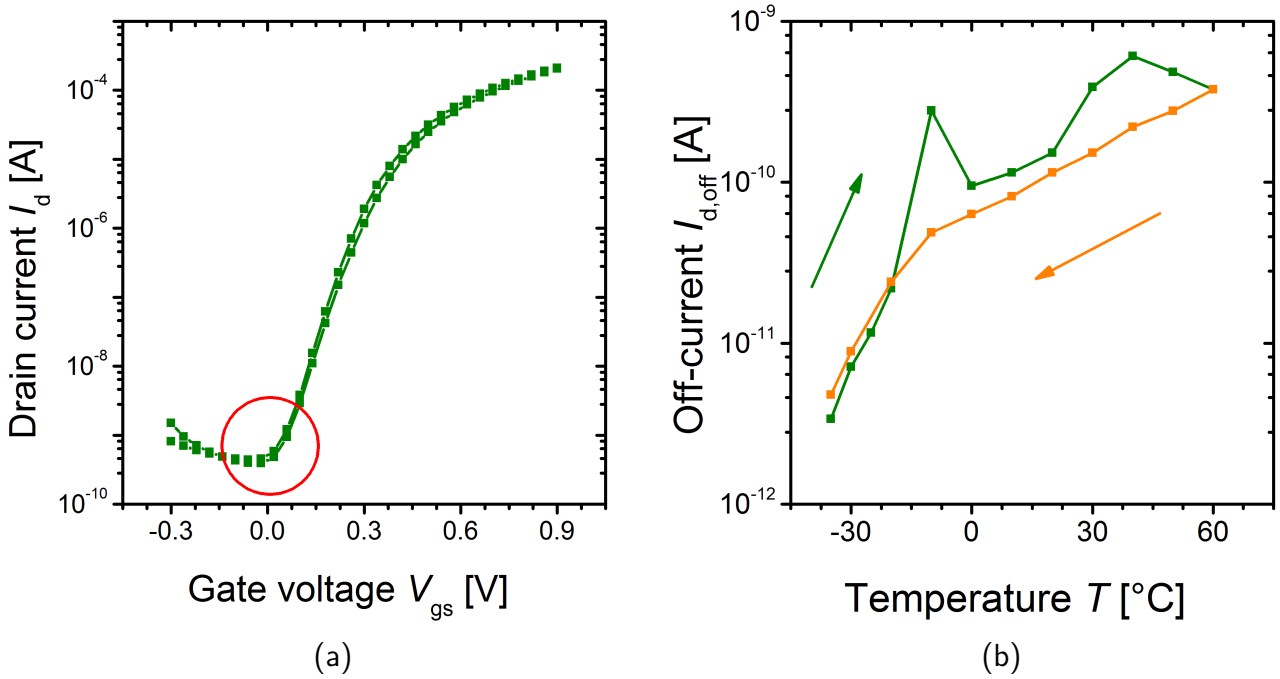


Figure 4.14.: (a) Exemplary transfer curve of an EG-FET with the indication of the off-current read off (red circle) and (b) the respective off-currents of an EG-FET as a function of temperature. The utilized current values are taken at $V_{gs} = 0.0\,V$ and $V_{ds} = 1\,V$

Figure 4.14(b) shows the temperature dependence of the off-currents $I_{d,off}$ in the off state with 0.0 V applied to the gate and 1.0 V applied to the drain electrode. The observed values vary between 3 and 600 pA for the investigated temperature range. The increase by more than two orders of magnitude is expected for an EG-FET, as for semiconductors the number of electrons in the conduction band increases with temperature, increasing the intrinsic conductivity.

On/Off-Current Ratio

The on/off-current ratio is an important characteristic parameters for device applications. Especially for digital circuits a large on/off-current ratio ensures a clear distinction between on and off state (or logic 1 and 0) in the circuit. Thus, the larger the current difference between on and off state, the better the transistor performance. Figure 4.15(b) shows the on/off-current ratio with respect to temperature. The value decreases with temperature by two orders of magnitude from $4{\cdot}10^7$ at -35 °C to $4{\cdot}10^5$ at 60 °C. This behavior is mostly driven by the change of the off-current shown in Figure 4.15(b). The on-current was found to be constant with temperature as will be

shown below. But even the value of the on/off-current ratio of $4{\cdot}10^5$ at the highest temperature is still sufficiently large to design functional digital electronic circuits.

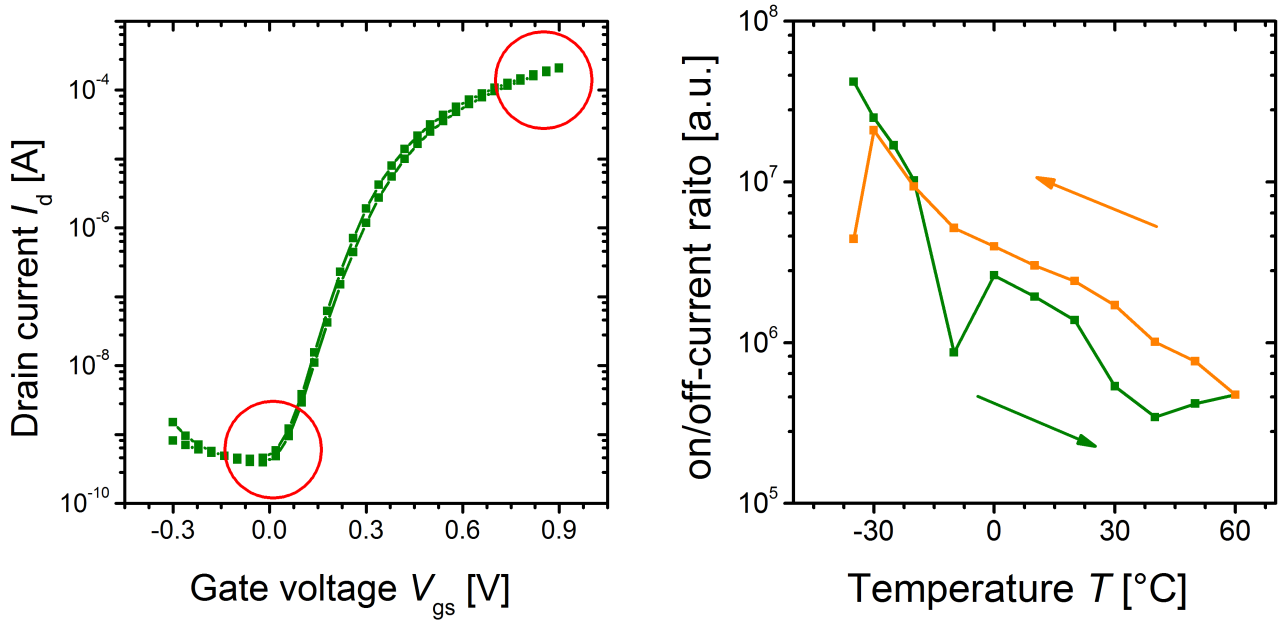


Figure 4.15.: (a) Exemplary transfer curve of an EG-FET with indication of the current values utilized to determine the on/off-current ratio (red circles) and (b) the on/off-current ratio of an EG-FET with respect to temperature. The values for the on-current are taken at $V_{gs} = 0.9\,V$ and $V_{ds} = 1\,V$. Those for the off-current are taken in accordance with Figure 4.14(b)

Subthreshold Swing

The subthreshold swing SS is the inverse of the subthreshold slope and is measured in the subthreshold region, which is located in the V_{gs} regime below the threshold voltage. SS is a measure for how much gate voltage is needed to change the drain current by one order of magnitude. A steep rise in a logarithmic plot of I_d with V_{gs} can be beneficial for low voltage and low current operation in digital circuits and memory applications. The SS is defined as

$$SS = \ln(10)\frac{dV_{gs}}{d\ln(I_d)} \tag{4.14}$$

From MOSFET calculations for inversion mode FETs the temperature dependence of SS is known to be

$$SS = \ln(10)\left(\frac{k_B T}{q}\right)\frac{C_{diel} + C_{depl}}{C_{diel}} \tag{4.15}$$

where C_{diel} is the areal capacitance of the gate dielectric and C_{depl} is the areal capacitance caused by the depletion layer in an inversion mode FET.

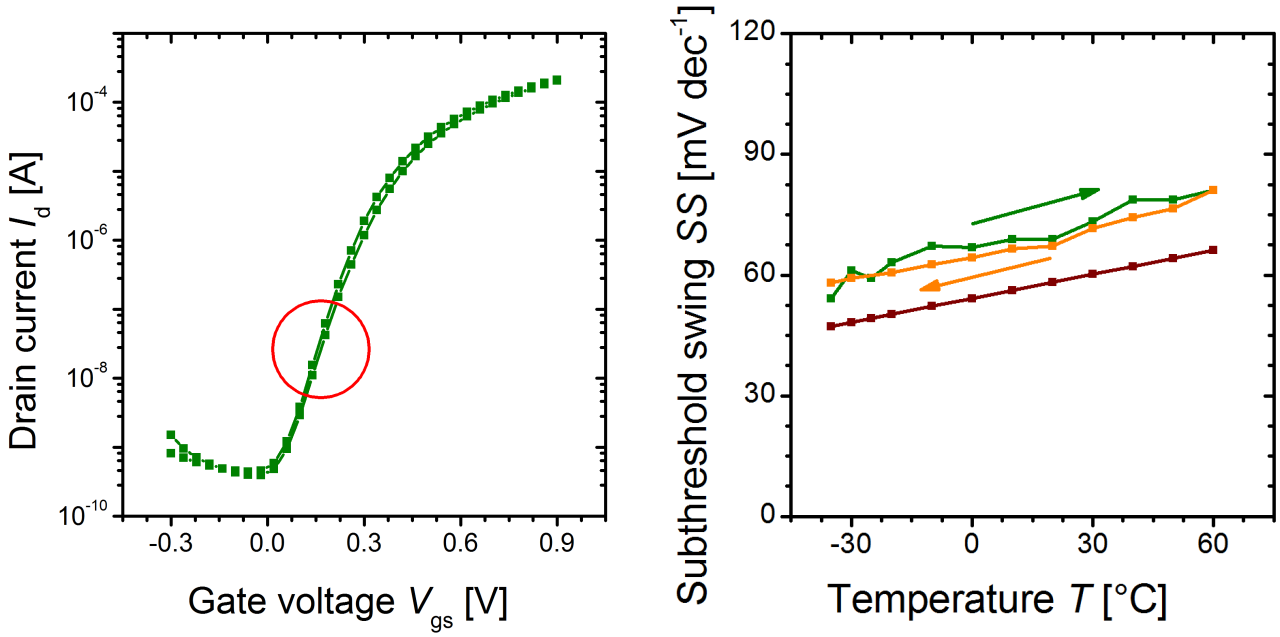


Figure 4.16.: (a) Exemplary transfer curve of an EG-FET with indication of the subthreshold region (red circle). (b) Subthreshold slope of an EG-FET and theoretical curve following eq. (4.16) (brown line) with respect to temperature. Values are measured in the V_{gs} window between off-current and V_{th}. In all measurements V_{ds} was set to 1 V.

In case of an accumulation mode FET, as investigated in this thesis, C_{diel} has to be replaced by C_{dl} and C_{depl} can be removed because no depletion layer is formed in an accumulation mode FET. With these adjustments eq. (4.15) is simplified to

$$SS = \ln(10)\left(\frac{k_{\mathrm{B}}T}{q}\right). \tag{4.16}$$

Figure 4.16(b) shows SS as a function of temperature and the theoretical prediction by eq. (4.16). The measured and calculated values exhibit the same slope, however, with a constant offset. The offset of the measured values from the theoretical minimum is also a measure for the interface trap states density at the semiconductor/CSPE interface [81]. Trapped charges at the interface can be represented by a trap related areal capacitance (C_{trap}), which modifies the areal double layer capacitance just like the areal capacitance above discussed caused by the depletion layer. Thus,

it can be included in the areal capacitance term in eq. (4.15) before simplification. The accurate description of SS reads then as follows:

$$SS = \ln(10) \left(\frac{k_\mathrm{B} T}{q} \right) \frac{C_\mathrm{dl} + C_\mathrm{trap}}{C_\mathrm{dl}}. \tag{4.17}$$

where C_trap accounts for about 20 % of the overall areal capacitance. It can additionally be used to estimate the trap density σ_trap using

$$C_\mathrm{trap} = \frac{q\,\sigma_\mathrm{trap}}{V_\mathrm{gs}}, \tag{4.18}$$

which results in $1.1{\cdot}10^{12}\,\mathrm{cm}^{-2}$. The small number of charge traps at the interface and the similarity of SS to an ideal slope in the subthreshold region promise a very good transition behavior and show the high quality of the prepared EG-FET.

Threshold Voltage

The threshold voltage is the gate voltage, where an ideal transistor switches on. It is defined as the value where the extended linear section of the square root curve of I_d (blue curve in Figure 4.17(a)) has to be zero. In an ideal transistor at $T = 0\,\mathrm{K}$ the subthreshold slope would be infinitely steep and the square root curve would exhibit a kink at the threshold voltage. The value of V_th is a crucial factor for circuit applications like inverters. It influences the design and functionality of digital circuits. A shift with changing temperature can compromise the functionality and must be known to be taken into account in the circuit design. Figure 4.17(b) displays the threshold voltage of the investigated EG-FET. The threshold voltage does not change substantially, in this case in the range of 0.2 V - 0.3 V.

Additionally, the trap density at the semiconductor/CSPE interface can be estimated from the threshold voltage. The areal trap density σ_trap can be calculated from the following equation

$$\sigma_\mathrm{trap} = \frac{C_\mathrm{dl} V_\mathrm{th}}{q} \tag{4.19}$$

which results in a trap density of σ_trap =$8.1{\cdot}10^{12}\,\mathrm{cm}^{-2}$. This number is quite small and is in the same order of magnitude as the value calculated using C_trap. Such a small number makes the temperature influence on the threshold voltage very small.

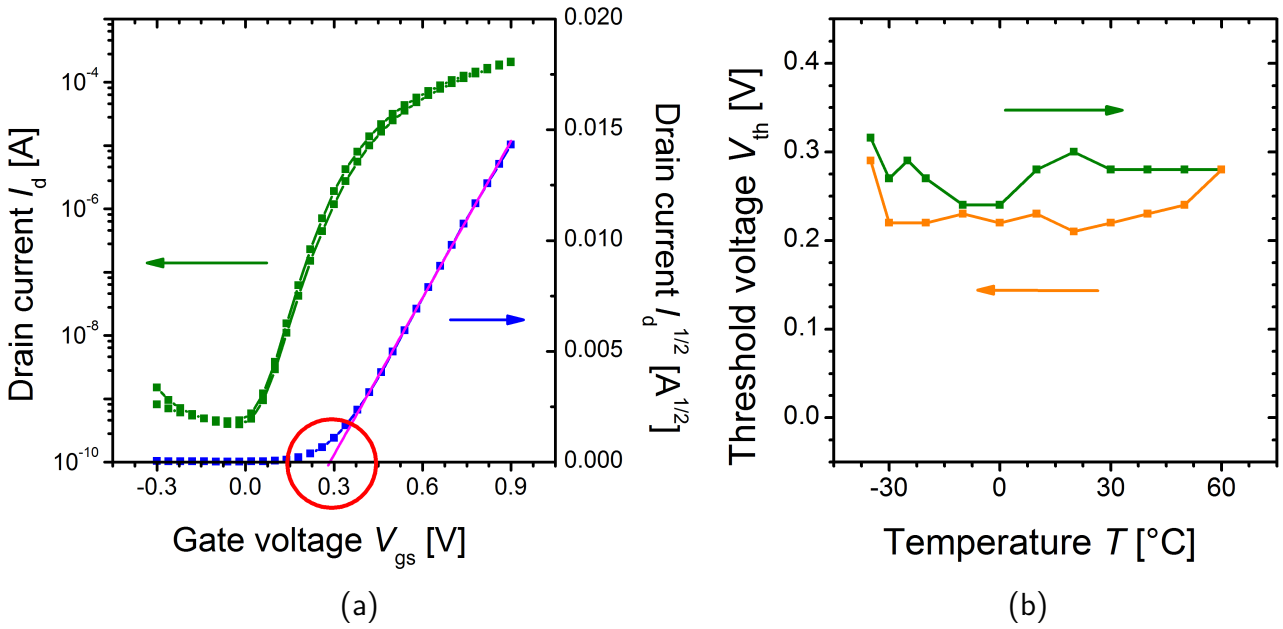


Figure 4.17.: (a) Exemplary transfer curve of an EG-FET with indication of the threshold voltage read off points (red circle) and (b) threshold voltage with respect to temperature. In all measurements V_{ds} was set to 1 V.

The trap states at the interface have to be filled before the charges, in this case electrons, can contribute to the channel formation. With increasing temperature the number of traps should reduce and the threshold voltage would reduce as well. Such a decrease with temperature cannot be clearly seen in Figure 4.17(b). This can have two reasons: 1) The traps are located energetically so deep, that the temperature change does not make a difference in their occupation, or 2) the number of traps is so small, that the effect of the trapped charges vanishes within the measurement uncertainty.

In comparison, silicon semiconductor theory predicts a reduction of the threshold voltage of about 1 mV/K due to a reduction of the band gap. For highly doped materials this value can shrink to 0.7 mV/K [82]. If a similar behavior is present for a material like In_2O_3 the effect on the threshold value would be even smaller due to a typical intrinsic carrier concentration of In_2O_3 of $\sim 10^{19}\,\mathrm{cm}^{-3}$. The resulting variation of V_{th} of < 70 mV can easily be within the error of tcirclehe determination method. Overall, the constant value of V_{th} with temperature is very beneficial for an application in everyday applications.

Field-Effect Mobility

The mobility is defined as the proportionality factor between the electron drift velocity v and the electric field E. Therefore, it yields $v = \mu E$. In the case of a field-effect transistor, the field-effect mobility not only influences the magnitude of the on-current, a higher μ_{FET} also enables a faster channel formation and a faster electron transit through the channel region whereby the latter

allows for a higher switching frequency. For example, in a series of FETs where a gate of one FET is charged by a current through another FET, the mobility determines the charging speed of the first FET. A high μ_{FET} is thus beneficial for a faster operation of such coupled devices. The field-effect mobility is determined as discussed earlier in section 3.1.8 from the slope of the square root function of I_{d}. Figure 4.18(b) shows the field-effect mobility measured for different temperatures. The decrease can be explained by the interaction of electrons with an increased number of phonons generated in the semiconductor with temperature. Following theory, the mobility change follows the equation $\mu_{\mathrm{Ph}} = C \cdot T^{-3/2}$ with μ_{Ph} the phonon modified mobility [83]. The experimentally determined field-effect mobility decreases from a value of $\mu_{\mathrm{FET}} \approx 120\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ at T = -30 °C to $74\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ at T = +60 °C. When the constant C is determined at T = -30 °C, a theoretical prediction for the decrease in carrier mobility due to increased phonon scattering can be calculated. The so calculated mobility values are shown in Figure 4.18(b), and plotted as a brown line.

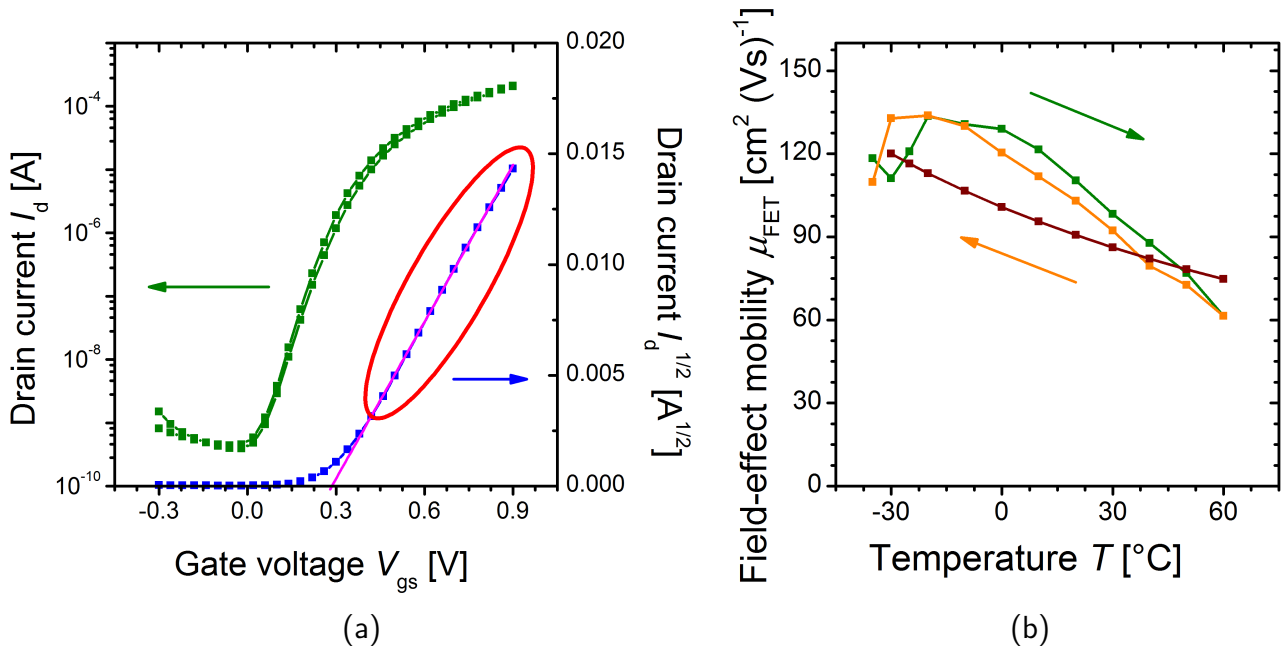


Figure 4.18.: (a) Exemplary transfer curve of an EG-FET with logarithmic plot of I_{d} (green) and the linear plot of $I_{\mathrm{d}}{}^{1/2}$ (blue) with indication of the region μ_{FET} is determined from (red ellipse). (b) Field-effect mobility of an EG-FET with respect to temperature. The values are calculated from the curves in the saturation regime with V_{ds} set to 1 V. Theoretical curve giving the temperature dependence of μ_{FET} influenced by phonon scattering (brown).

It can be seen that the overall temperature dependence is satisfactorily represented by the brown line in Figure 4.18(b). The reason for the observed deviations is presently not understood.

On-Current

The on-current is the current in the saturation regime that can be carried by the semiconductor channel for $V_{gs} - V_{th} > V_{ds}$ and in this case read off at $V_{gs} = 0.9\,V$. In an electric circuit this current determines how fast a capacitor or the gate capacitance of another FET can be charged. The higher I_d is, the faster a circuit can operate. A constant value of I_d with temperature therefore guarantees a constant operation speed of an FET. Figure 4.19(b) displays the saturated on-current as a function of temperature. One observes that the magnitude of the on-current does not change significantly over the investigated temperature range. This behavior becomes obvious when eq. (2.10) is analyzed carefully for the examined system. With a fixed geometry and V_{th} being temperature independent (see Figure 4.17(b)), C_{dl} and μ_{FET}, determine I_d in the saturation regime. The trend of the critical properties can be seen in figures 4.10(b) and 4.18(b). These two properties have opposing temperature dependencies and compensate each other, which results in a constant on-current. This also explains the trend of the on/off-current ratio (see section 4.2.2) since in this case its temperature dependence is solely determined by the off-current.

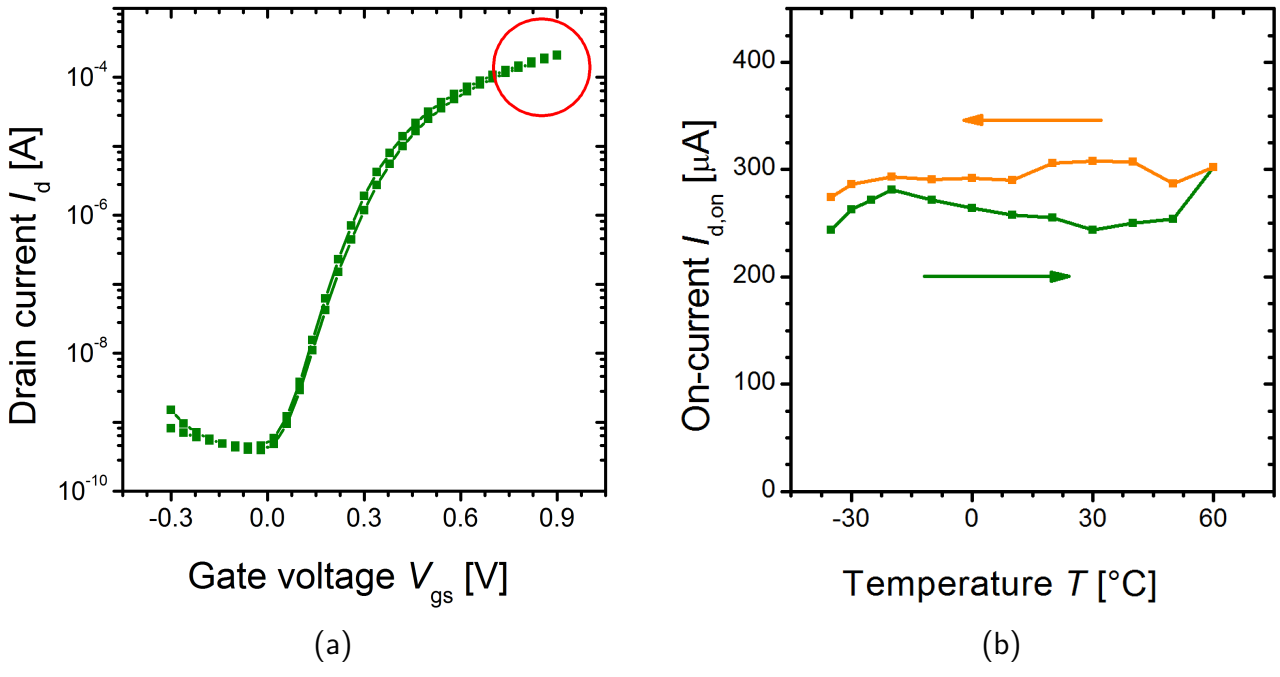


Figure 4.19.: (a) Exemplary transfer curve of an EG-FET with indication of the on-current read off region (red circle). (b) on-current of an EG-FET measured at $V_{gs} = 0.9\,V$ with respect to temperature. V_{ds} was thereby set to 1 V.

With the knowledge about the material and transistor characteristics, an analysis of the time constants of the EG-FET can be performed. There are basically two time constants that have to be considered:

- the transit time τ_{transit} for the electrons to cross the channel from source to drain and
- the time constant τ_{RC} necessary to form the electrical double layer and thus the conducting channel.

The first one is determining the maximum switching frequency of the transistor when already on and the second one is influenced by the properties of the electrolyte.

As stated in sections 2.2.1 and 2.3.2 the transit time $\tau_{\text{transit}} = L^2/\mu_{\text{FET}}V_{\text{ds}}$ is the time electrons need to travel through a semiconductor channel from source to drain with the channel length L, the field-effect mobility of electrons in the semiconductor μ_{FET} and the applied drive voltage V_{ds}. This transit time can be interpreted as the minimum switching time of the transistor in the on state. The switching time is calculated with μ_{FET} instead of the material related mobility μ_0, because in an FET the transit time includes the transfer of the electron from the source into the channel and from the channel into the drain electrode.

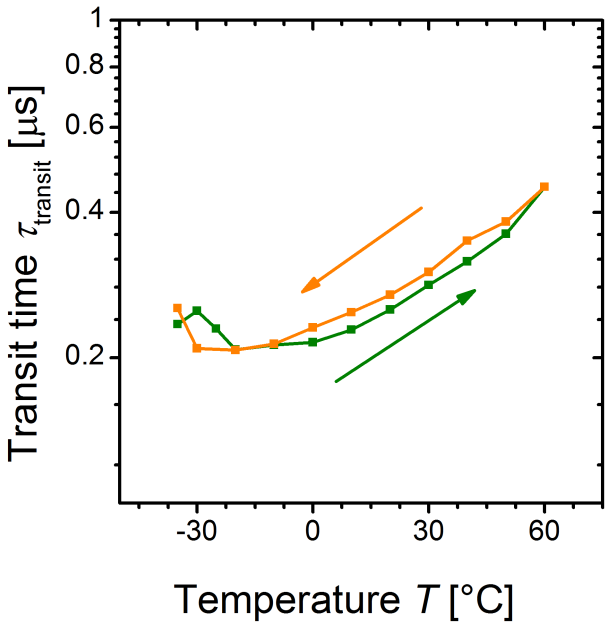


Figure 4.20.: Transit time τ_{transit} of an electrolyte-gated field-effect transistor with a channel length of 50 μm and a gate voltage V_{gs}= 0.9 V.

In addition, the charge carriers move in a narrow channel close to the dielectric and are influenced by the interface quality. This device specific conditions are automatically implemented when using the field-effect mobility μ_{FET}. Figure 4.20 displays the trend of τ_{transit} with temperature

and suggests minimum switching times of $<1\,\mu$s, which corresponds to a cut-off frequency of >1 MHz. With temperature, the transit time increases due to the decrease of μ_{FET}. The second time constant determining the switching speed is the time, which the ions in CSPE-1 need to form the electrical double layer. The charging time of C_{dl} can be described by the time constant τ_{RC} of the involved RC circuit as described in section 2.3.1 (see Figure 2.12). It can be calculated from $\tau_{\mathrm{RC}} = R_{\mathrm{CSPE}} \cdot C'_{\mathrm{dl}}$ with R_{CSPE} determined from the electrolyte conductivity σ_{el} and the electrolyte geometry and the double layer capacitance C'_{dl} of the semiconductor/electrolyte interface.

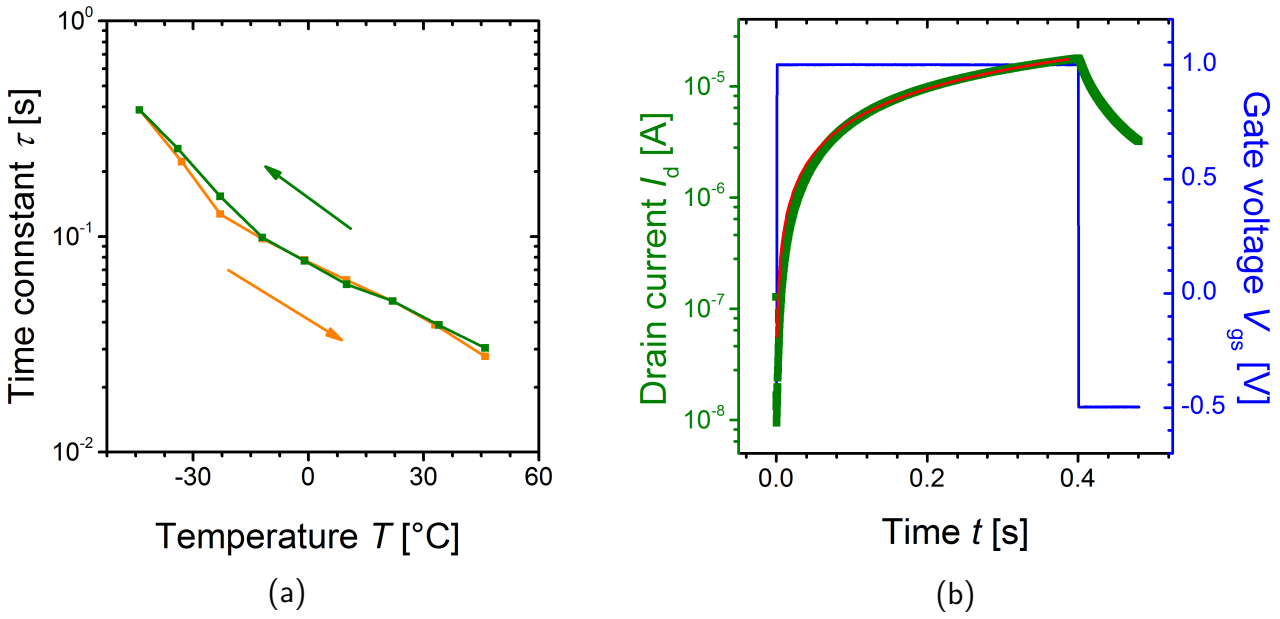


Figure 4.21.: (a) Time constant τ_{RC} of a CSPE filled capacitor calculated from the product of the double layer capacitance and the ionic conductivity with respect to temperature. (b) Experimental verification of the time constant of an in-plane EG-FET with fitted exponential function for determination of the time constant τ_{RC} with V_{ds} set to 1 V.

Figure 4.21(a) shows τ_{RC} as a function of temperature. The time constant for the formation of the electrical double layer varies in the range of 0.03 s to 0.4 s and is much longer than τ_{transit}. The examined device speed for switching is thus limited by the ionic conductivity σ_{el} and the double layer capacitance C'_{dl}. An experimental determination of the time constant τ_{RC} of an EG-FET with the same geometry was performed by applying a voltage step to the gate of an EG-FET at room temperature. The utilized experimental parameters are displayed in Figure 4.21(b) and the fit function is represented by $I_{\mathrm{d}} = A \cdot (1 - \exp(-t/\tau_{\mathrm{RC}}))$ with A the maximum value for I_{d}. By fitting of an exponential function to the measured drain current a time constant of $\tau \sim 1$ s is extracted. This value is about one order of magnitude higher, than the calculated time constant at room temperature. The discrepancy can be explained by a certain difference between the bulk conductivity of a CSPE in a parallel plate capacitor and the thin film like appearance in the geometry of an in-plane field-effect transistor. It can be concluded that for the film thickness of

about 1 μm of CSPE-1(sd) and the high surface to volume ratio changes the solidification behavior and reduces the amount of solvent/plasticizer in CSPE-1.

Another point of interest is the observed hysteresis of the transfer curves at low and high temperatures shown in the appendix C. It is obvious that a hysteresis appears in the transfer curves for the two extreme temperature regions, ranging from 50 °C to 60 °C and from -20 °C to -35 °C. At low temperatures this process can be explained by the increased time constant τ_{RC}. Because all experiments were conducted with the same setting of the sweep rate to make them comparable, the electrolyte may not have been in a steady state at low temperatures. This interpretation is likely since the hysteresis vanishes with the introduction of waiting times of 5 seconds following each voltage step. The waiting time is introduced after the change of voltage at the gate electrode to allow the proper formation of the electrical double layer. Figure 4.22 shows a transfer curve of an EG-FET without waiting time (purple) and with waiting time (orange). It has to be mentioned that the increase of τ_{RC} for low temperatures can also be the reason for the decrease of μ_{FET} at -35 °C (see Figure 4.18(b)). For high temperatures the hysteresis can be due to dynamic effects within CSPE-1. More scattering due to higher ion energies correlated to higher velocities of the species could be one possible reason. However such an assumption definitely needs proof and is therefore purely speculative.

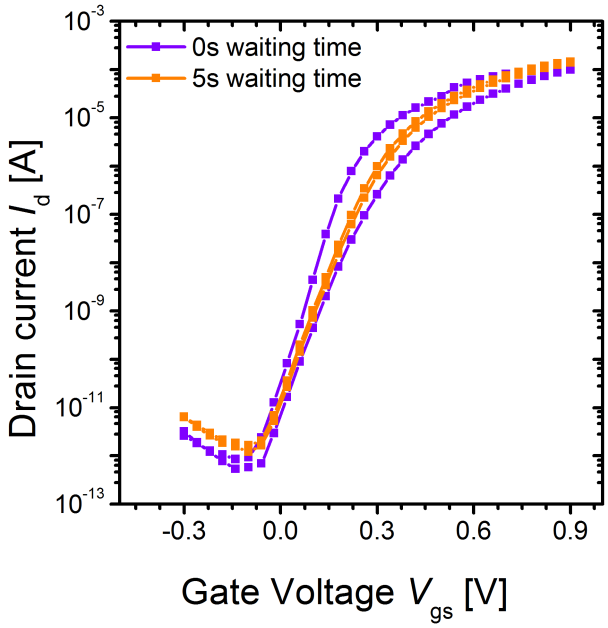


Figure 4.22.: Transfer curves of a CSPE gated FET at -30 °C with V_{ds} set to 1 V. The waiting time after voltage (V_{gs}) change is 0 s (orange) and 5 s (purple).

4.3 Mechanical Properties of CSPEs

As stated earlier, printed electronics and the use of flexible substrates are closely related. For future applications of CSPEs such flexible substrates would be a necessity to enable roll-to-roll

processing and to keep the cost down. To show the principle suitability of flexible substrates in conjunction with printable electrolyte based electronics, some mechanical properties of the CSPEs are investigated. Rheology measurements are performed to understand the physical state as well as the viscosity of the CSPEs. Tensile stress tests are supposed to give information about the ultimate stress a CSPE can withstand.

4.3.1 Rheological Properties

Rheological measurements are performed to gain insight into the viscoelastic properties of the CSPEs. As the most promising system CSPE-1 is analyzed during the solidification process as well as its temperature dependence in the solid state. Figure 4.23 shows the change of storage and loss modulus during the solidification process of CSPE-1 over 60 h. The storage modulus represents the amount of energy stored inside the material during a controlled rotation. The loss modulus represents the amount of energy, which is lost due to irreversible deformation and generated heat.

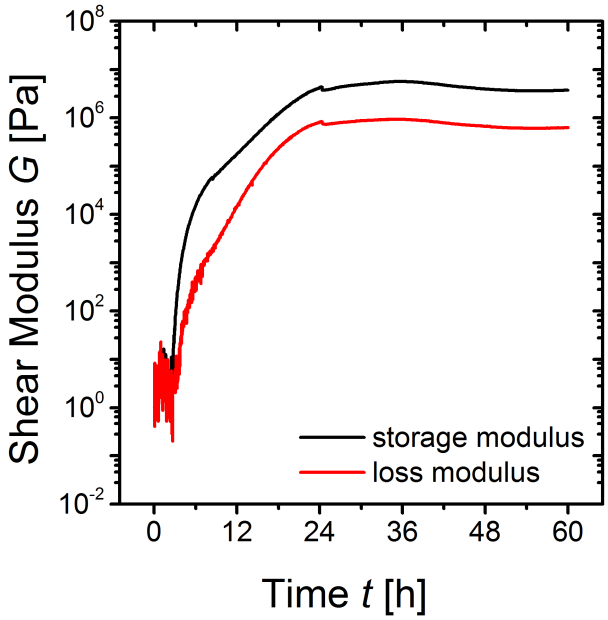


Figure 4.23.: Storage (black) and loss (red) modulus of CSPE-1 during solidification. The solidification is conducted under a constant flow of dry air (200 sccm) for 60 h.

As can be seen from Figure 4.23 the solidifying electrolyte changes its properties with time and finally reaches a stable state. In the first five hours the material shows moduli of ∼1 Pa for both storage and loss modulus and is considered liquid. Afterwards both values increase, which indicates the onset of polymerization of the PVA. With the evaporation of solvent (and plasticizer) and the ongoing cross-linking of the polymer chains in the material gain more and more physical stability and the moduli increase. After about 25 h a stable state is reached in form of a strong gel. A strong gel is a state, which shows a large storage modulus compared to its loss modulus

meaning that only a small portion of the rotational energy input is lost, whereas the major part of the energy is stored and regained during the reverse rotation. In this stable state the temperature dependent measurements were conducted. Figure 4.24 shows the change of storage and loss moduli with temperature. One can clearly see a decrease of both moduli with temperature. The trend of the storage modulus is representing a softening of CSPE-1(sd) towards high temperatures. The ratio of storage to loss modulus changes from 90:10 to 80:20 from low to high temperatures. Where at -40 °C only about 10 % of the energy is lost, at 50 °C almost 20 % are lost to deformation or heat. The measurement indicates a reduced structural strength and a reduced viscosity at high temperatures. Still, at any temperature the material can be considered a strong gel.

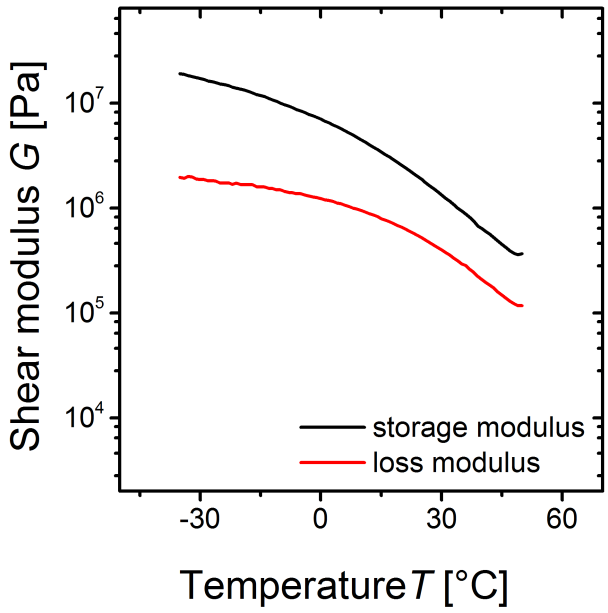


Figure 4.24.: Rheological measurement of CSPE-1(sd) in a temperature range between -40 °C and 50 °C.

4.3.2 Tensile Strength

With the knowledge of the physical aggregate state from the rheology measurements and the presence of liquid components in the CSPEs(sd) from the composition analysis in section 4.1.1 the tensile strength of the material is investigated. The measured strength is compared to the strength of solid polymer electrolytes from literature. Figure 4.25 shows the behavior of a CSPE-1(sd) film under tensile stress. The tensile stress increases until a strain of about 20. The increase is not linear, which indicates irreversible deformation from the beginning of the stretching. A purely elastic/reversible behavior would be indicated by a linear slope of the stress-strain curve. As seen in rheology data, the behavior of CSPE-1(sd) is not purely reversible (storage modulus) but has an irreversible component (loss modulus) even for very small deformations. With further elongation the tensile stress is increasing with a much lower incline. At a maximum stress of 5 MPa and

a strain of ∼63 the sample ruptured. The value of maximum stress obtained is comparable to other solid polymer electrolytes. Niitani et al. show tensile strength of ∼15 MPa for a block-co-polymer/$LiClO_4$ mixture [84], Zhao et al. showed a tensile stress of ∼3 MPa with a mixture of PVA and H_3PO_4 [85] and Kelly et al. showed ∼1 MPa with a mixture of PEO and $LiClO_4$ [86].

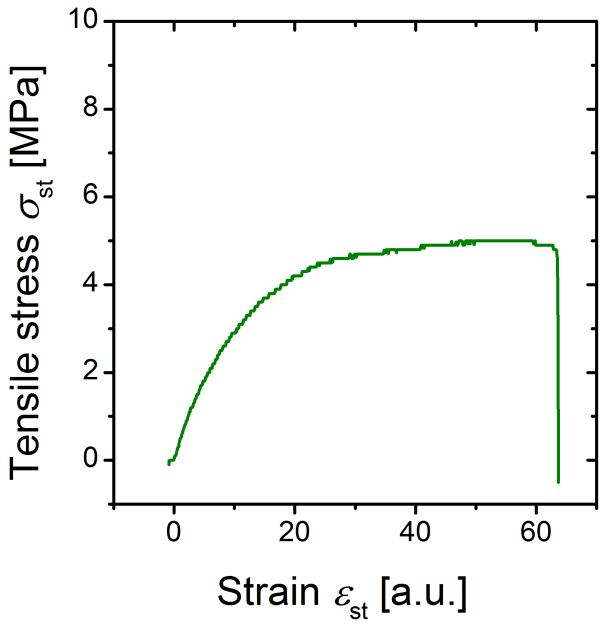


Figure 4.25.: Stretching behavior of a solid CSPE-1 film in a micro tensile test device until rupture.

All these components are considered solid. The mechanical properties for CSPE-1(sd) are very promising for its use on flexible substrates for future applications.

4.4 Summary

In this chapter CSPEs as replacements for conventional dielectric materials in FETs are investigated. The compositions of three CSPEs are investigated and their phase does not change in a large temperature range (-30 °C to 50 °C). By means of impedance spectroscopy the electrical properties like electrolyte conductivity and areal double layer capacitance are investigated with respect to temperature. The trends with respect to temperature of the respective quantities is shown and described by a theoretical model. The most suitable candidate in terms of conductivity, areal capacitance and printability was selected, and introduced in printed CSPE gated field-effect transistors. These FETs were investigated with respect to temperature and the characteristic values such as on-current, on/off-current ratio, subthreshold slope, threshold voltage and field-effect mobility were extracted from transfer and output characteristics for the respective temperatures and interpreted by classical theory. Constant values for threshold voltage and on-current could be shown and, in general, a very stable performance of the EG-FET was observed. The time constants τ_{transit} and τ_{RC} were determined and the weakness in terms of switching speed and

the need to find new geometries to reduce the dominant time constant of the system are pointed out. This problem will be tackled in the following chapter, which reports on a new vertical FET structure involving porous semiconductor morphology and a new way of realizing a back-gated channel device. Finally, the physical state and mechanical strength were tested and indicated the suitability of CSPE-1(sd) for future application even on flexible substrates.

5 Printed Porous Channel EG-FETs

In this chapter a new approach to realize a vertical channel FET (v-FET) is presented. It relies on a combination of the stacked channel strategy proposed by Yu et al. [67], using a stacked "source-channel-drain" (from bottom to top) structure and the wrapped channel solution shown by Ng, Egard and Tomioka [64–66], in which vertically aligned nanowires with a dielectric and a gate electrode have been proposed. This combination has been accomplished by stacking a printed porous semiconductor between two metallic electrodes, i.e., source and drain. The gating is then made by infiltration of CSPE into the entire semiconductor network completely wrapping the semiconductor with CSPE and, additionally, by contacting a gate electrode with the CSPE. The aim is to overcome the usual lateral printing resolution of $\sim$10 μm, reduce the channel length to 50 - 100 nm and reach high current densities with minimized device geometries. Furthermore, the potential of such materials for applications at high frequencies will be shown.

To realize this concept, a SnO_2 precursor ink containing micelles forming polymers to ensure the porous structure of the semiconductor is developed. The composition and calcination routine of the precursor is optimized and the final product is analyzed by means of optical and refractive methods. Vertical FETs with different geometrical dimensions have been constructed with porous SnO_2 as channel material and are electrically characterized. To estimate the relevant physical parameters, practical approximations are introduced, which display the porous semiconductor as pillars to calculate the surface area and areal capacitance. To gain more profound insight into the functionality of the porous semiconductor network in a v-FET, simulations are performed, which suggest possibilities for further optimization of the device. Finally, to overcome the low switching speed of displaced gate EG-FETs, a back-gated EG-FET is constructed, where the porous channel and the gate located below, are separated by a printed film of porous Al_2O_3.

5.1 Functional Principal of Vertical FETs

The v-FET consists of a stacked source/channel/drain structure with a laterally displaced gate as schematically displayed in Figure 5.1. After preparation of the bottom electrodes, i.e., source and gate by electron beam lithography and radio frequency sputtering, a mixture of Sn-salt ($SnCl_4$), solvents (ethanol and water) and an ambipolar micelles forming polymer, from now on referred to as SnO_2 precursor is applied using inkjet printing. The top electrode. i.e., drain is also prepared by electron beam lithography and radio frequency sputtering on top of the dried SnO_2 precursor. After a calcination step to finalize the formation of the porous semiconductor structure CSPE-1(lq) is printed onto the channel and gate area. The CSPE(lq) then infiltrates the porous

network and contacts physically and electrically the entire semiconductor surfaces. This principle allows CSPE-1(sd) to address the entire surface of the semiconductor network, which can be used as FET channel.

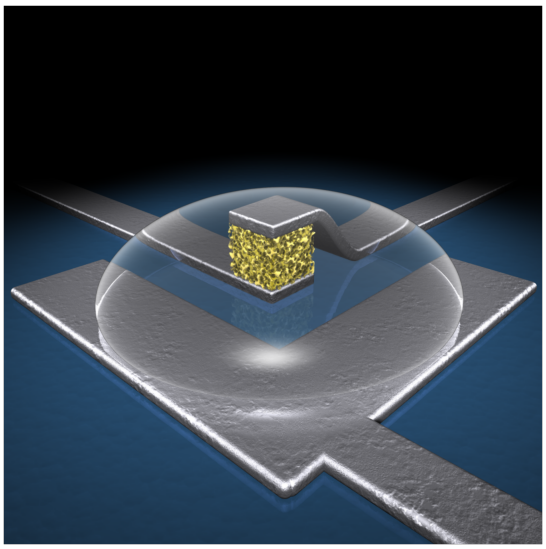


Figure 5.1.: Schematic of a vertically aligned porous channel EG-FET.

One advantage of the present approach compared to other printed FETs is that the channel length is not limited by the lateral printing resolution of commercial printers, which is usually in the range of 10 - 20 μm but rather by the thickness of the printed layer. Thereby the channel length of 10 - 20 μm of an in-plane FET, which is given by the spatial printing resolution can be overcome. With this device structure it is possible to reduce the channel length to < 50 nm and reduce the channel length by almost three orders of magnitude. The porous semiconductor is still the crucial part of the FET. The right porosity and semiconductor properties are required for a proper functionality of the device. Different preparation routines are tested and the one showing the best device performance is characterized in more detail. Still, a complete infiltration of CSPE-1(lq) into the pores of the channel is desirable to obtain the most efficiently working devices.

5.2 Preparation and Characterization of Porous SnO_2

In order to prepare the porous SnO_2 semiconductor an SnO_2 precursor is utilized, whose composition was published before [74]. The SnO_2 precursor is then printed, dried and calcined. Different polymers and calcination parameters are used to obtain various porous morphologies of the semiconductor. From principle considerations there should be three main factors determining the pore size in the semiconductor: first, the chain length or degree of polymerization of the added ambipolar polymer, second the calcination temperature and third the calcination time. The chain length

of the added ambipolar polymer should, in principle, determine the size of the micelles, which are formed during the evaporation of the solvent. During this drying process, the reducing solvent in the SnO_2 precursor leads to stronger precipitation of micelles due to a more and more saturated polymer solution. The diameter of the micelles relates to the chain length of the polymers. In the drying SnO_2 precursor the micelles arrange themselves in the form of chains of connected individual micelles, which form a continuous network. This network forces the simultaneously drying SnO_2 precursor into the space between the micelles, thus forming a complementary network of solidified SnO_2 precursor. It has to be noted that both are in the solid state. At increased temperatures of around 400 °C the polymer starts to decompose, leaving the sample as a gas. The thereby generated air filled pores establish a network of interconnected and solidified SnO_2 precursor-salt in the form of filaments. In the present thesis two different ambipolar polymers of different chain lengths have been tested. One of them is an ambipolar polymer, referred to as KLE, which is a block copolymer with two components consisting of 89 monomeric units of ethylene-co-butylene and 79 monomeric units of ethylene oxide as can be seen in Figure 3.6(a). The other, referred to as PIB-*b*-PEO, is also a block copolymer with two components consisting of 107 monomer units of isobutylene and 150 monomeric units of ethylene oxide separated by a phenyl ring as shown in Figure 3.6(b) (see section 3.2.2). According to the chain length a larger pore size or inter-filament distance is expected for the the SnO_2 precursor with PIB-*b*-PEO. The second and third parameters to influence the pore size are the time and temperature of the calcination process, respectively. The principle function of the calcination is the conversion of the solidified SnO_2 precursor ink into crystalline SnO_2. The crystallization process starts between 450 °C and 500 °C when heated up at a constant heating rate of 10 °C min^{-1} as shown below by XRD studies. Different calcination temperatures are applied for different holding times and result in different morphologies. The longer a sample is calcined the larger the width of the SnO_2 filaments becomes. During the crystallization process $SnCl_4$ is converted to the desired SnO_2 whereby initially created nanocrystals start to grow and sinter. In the case of a porous material this means that diffusing atoms increase the filament width and reduce the pore size. Thus, a sample calcinated for longer times develops thicker semiconductor filaments at the expense of the pore size. Thereby the calcination temperature determines the diffusion speed. An elevated calcination temperature has an even stronger effect on the SnO_2 crystal formation than an increased calcination time since the diffusion coefficient is growing exponentially with temperature and the crystallite size square-root dependent on time. The calcination time and temperature is not exclusively determining the final porous SnO_2 filament and pore size but also the final crystallite size and quality as well as the doping level of the semiconductor. The latter is defined by the number of oxygen vacancies in porous SnO_2. The combination of ligament width, pore size, crystal size and doping level finally determines the performance of the semiconductor network as a channel material for an EG-FET.

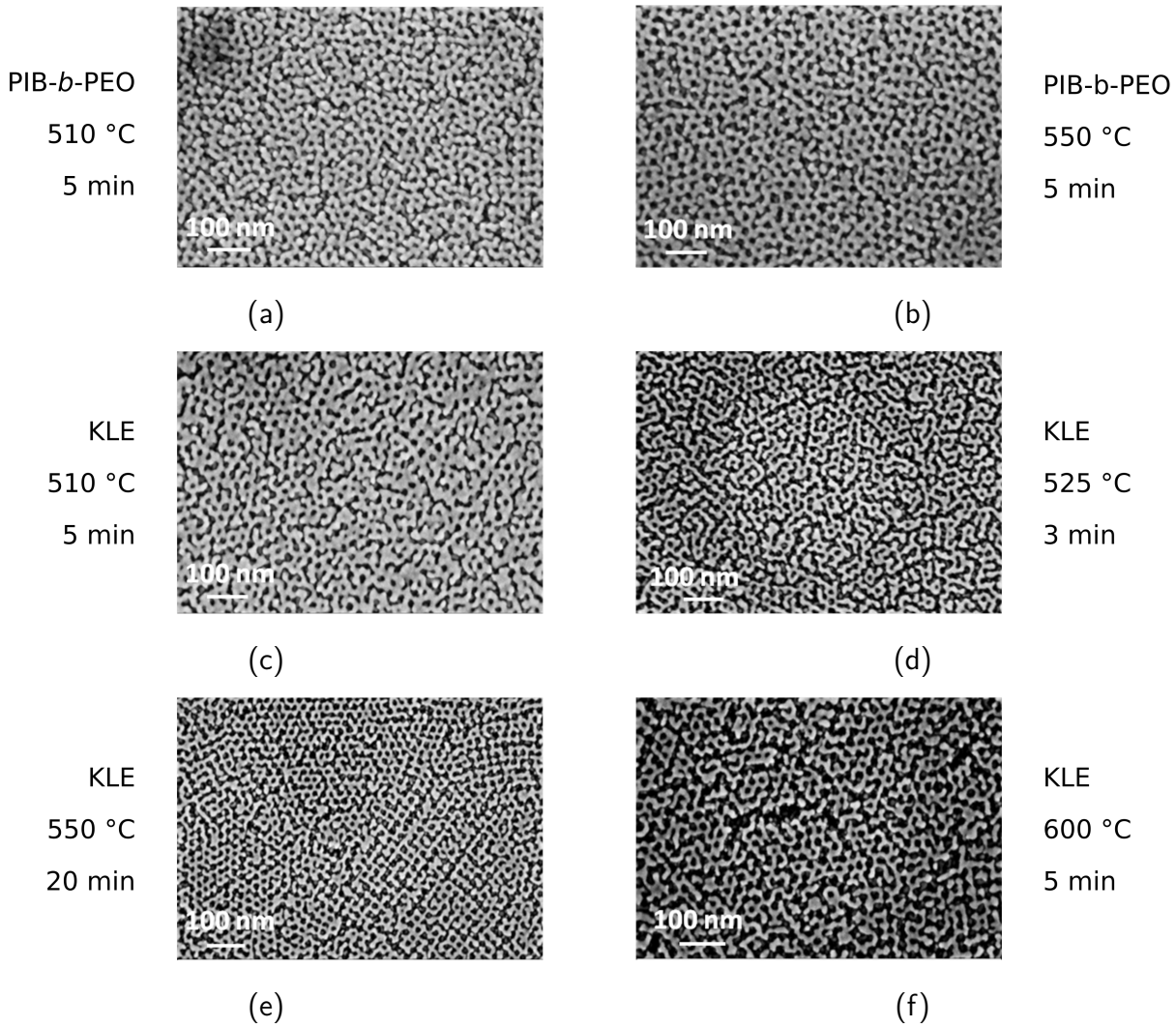


Figure 5.2.: SEM micrographs of the surfaces of two printed SnO_2 precursor inks calcined using different temperatures and times as indicated next to the respective micrographs.

For the characterization of the differently prepared porous SnO_2 films, SEM micrographs are taken to visualize the different morphologies. Figure 5.2 displays the SEM micrographs of the two different precursors calcined at different temperatures and for different times. It clearly indicates that the variation of temperature and time in combination with the use of different polymers generates different channel and pore morphologies. In these micrographs the white areas are the semiconductor and the black areas the empty pores. Figure 5.2(a) and 5.2(b) show porous SnO_2 films prepared with the longer polymer chain PIB-*b*-PEO. Figures 5.2(c) to (f) show samples prepared with the shorter polymer chain KLE. The pore sizes is expected to be wider for the porous SnO_2 prepared with the longer chain polymer PIB-*b*-PEO compared to the samples prepared with KLE. Experimentally, the size difference of the pores for the two precursor solutions is found, however, small after calcination. The reason for this observation most likely can be seen in the calcination process. Comparing figures 5.2(a) and (b) or 5.2(c) with (d) to (f), one can clearly see the influence of the calcination time. The longer the calcination time the thicker the SnO_2

filaments become resulting in a smaller width of the pores. As expected, the temperature has an stronger influence on the pore size as can be seen in figures 5.2(e). With increasing temperature the pores initially become smaller while at higher temperatures the pores (at the surface) become larger (see Figure 5.2(f)). This unexpected phenomenon is observed for the sample treated at 600 °C for 5 min. Apparently, at this temperature the sample shows again wider pores than the other samples, which indicates, that several factors are influencing the final product. The reason may still be seen in the above described process. Following the idea of sintering, the material to fill the pores in the bulk is taken from the sample surface and transported into the bulk of the sample. Such a process will widen the pores at the surface of the structure at the expense of the SnO_2 filament width. In addition, this sample experiences cracks, which most likely are caused by a fast cooling rate. Large temperature drops trigger the formation of cracks in the material due to thermal stress. Such cracks would strongly reduce the number of electrical percolation pathways from source to drain and thus compromise the device performance.

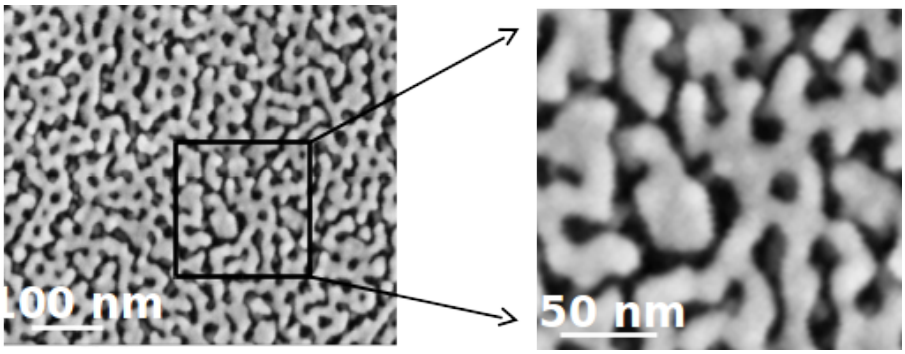
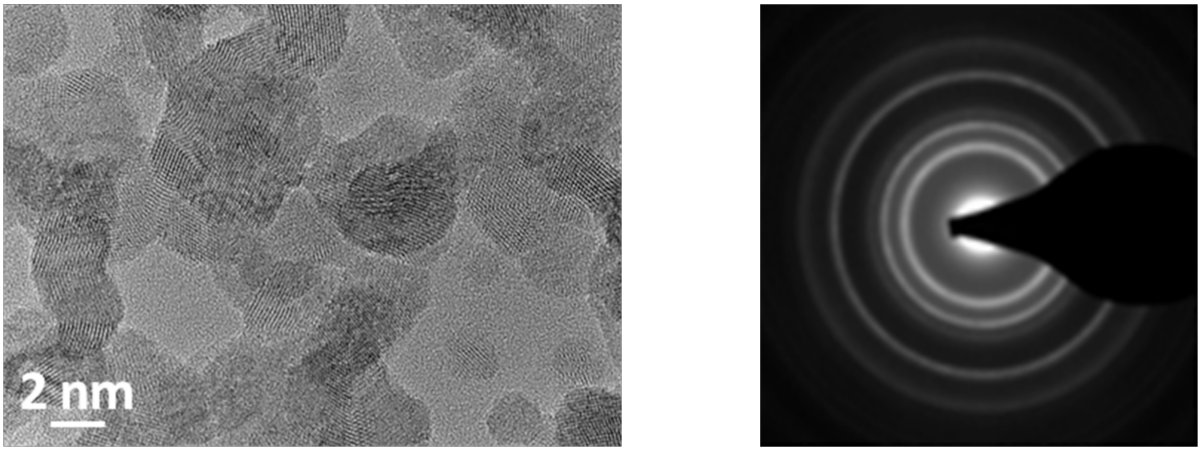


Figure 5.3.: SEM micrograph of a printed SnO_2 precursor ink calcined at 550 °C for 5 min with subsequent quenching at room temperature (left). An amplified image from the indicated area in (a) is shown on the right.

The best results in terms of FET-performance are observed for samples prepared with KLE heated to a temperature of T=550 °C and kept at this temperature for 5 minutes. An SEM micrograph of the material is shown in Figure 5.3. For such a morphology the infiltration with the composite solid polymer electrolyte works very well and no short circuits due to crack formation are observed. In the following these preparation conditions are applied to all v-FETs described in the present chapter.

To understand the structure and crystallinity of the porous film in more detail transmission electron microscopy (TEM) micrographs are taken. A printed and calcined film is prepared on a TEM grid with free standing 25 nm thick silicon nitride windows. The high resolution TEM micrograph (see Figure 5.4(a)) shows the nanocrystalline nature of the porous SnO_2. The regions not showing any crystallinity represent the empty pores.



(a) (b)

Figure 5.4.: (a) High resolution TEM micrograph of a porous porous SnO_2 filament calcined at 550 °C for 5 min indicating a polycrystalline structure with particle sizes of 3 - 5 nm and (b) SAED pattern which confirms the polycrystalline structure of the porous SnO_2 filaments.

In addition to the nanocrystalline structure in Figure 5.4(a) the SAED pattern in Figure 5.4(b) indicates the nanocrystalline nature of the porous SnO_2. Further proof for the degree of crystallization is provided by grazing incidence X-ray diffraction (GIXRD). Figure 5.5 shows GIXRD patterns of porous SnO_2 films calcined for 5 minutes at the indicated temperatures.

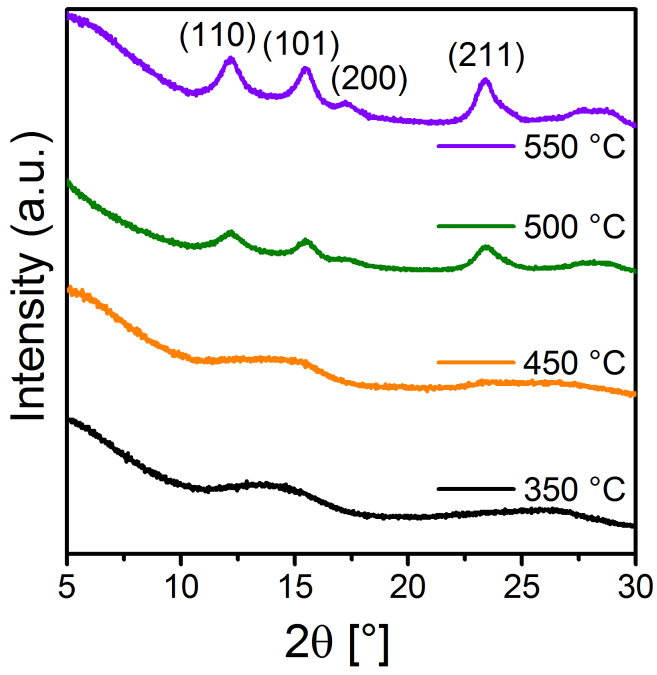


Figure 5.5.: Grazing incidence X-ray diffraction pattern of porous SnO_2 films calcined at indicated temperatures for 5 minutes.

Whereas for the calcination temperatures of 350 °C and 450 °C only amorphous structures are obtained the first crystalline domains can be detected at 500 °C. The reflections seen for the 550 °C calcined sample thereby corroborates nicely the SAED pattern from Figure 5.4(b).

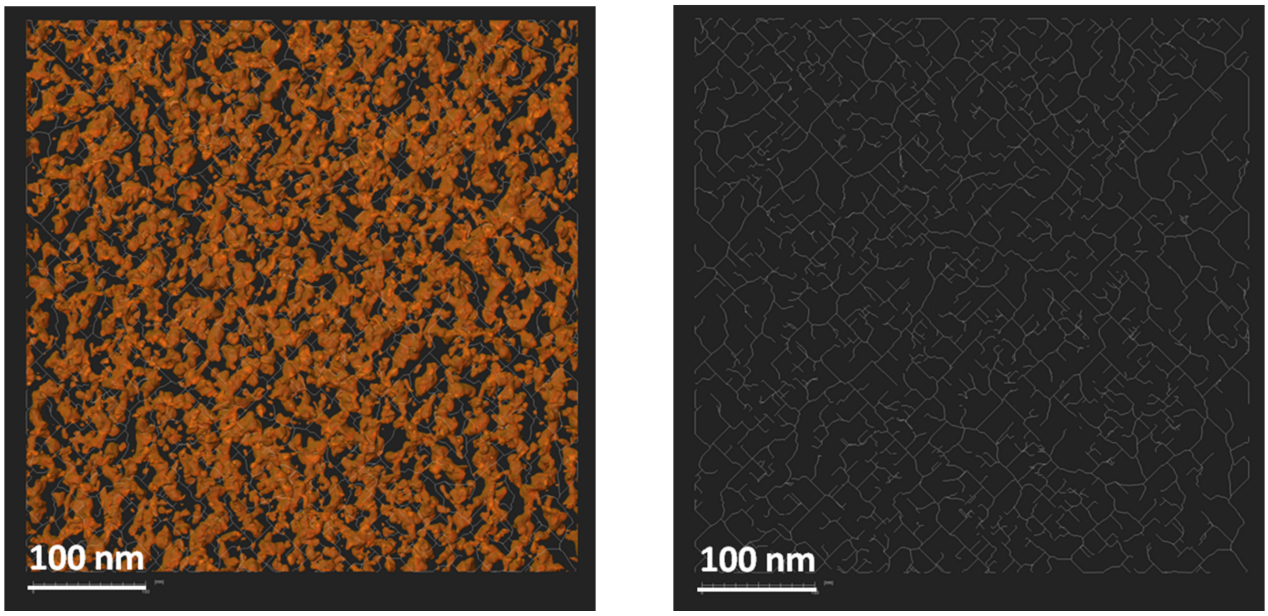


Figure 5.6.: (a) Reconstructed electron tomography image of the printed porous SnO_2 film and (b) computation of a skeletonization of the pore network showing the interconnections between the pores.

With increasing temperature the crystallinity increases, which can be seen from the more pronounced reflections at 550 °C. The crystallinity of the samples is mandatory for a proper function as semiconductor channel. The individual crystal size thereby influences the electrical properties of the semiconductor. An increased crystallite size results in a smaller number of grain boundaries, which reduces the scattering of charge carriers, in the present case electrons. Such reduced scattering increases the charge carrier mobility and the performance of the device. To utilize the full capability of such semiconductor networks in EG-FETs the entire surface of the porous SnO_2 semiconductor has to be addressed by CSPE-1(sd) through the pores. This enables, upon application of the gate voltage, the formation of the conducting channel of the field-effect transistor. Thus, it is essential to have a well-connected network of pores, in which CSPE-1(lq) can infiltrate and subsequently solidify.

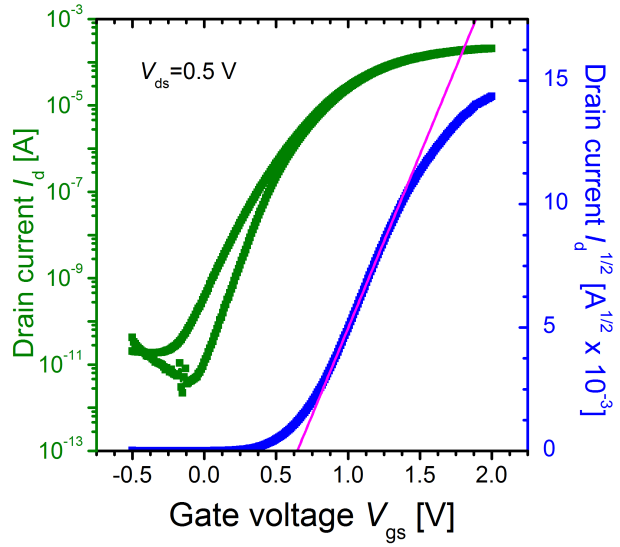
To check the accessibility of the inner surfaces of the porous SnO_2 network, an electron tomographic study is performed. For this technique the sample is rotated in a TEM in steps of 1 ° with respect to the electron beam, while scanning TEM images are taken at every position. A tomographic algorithm is used to reconstruct the 3d image of the examined material. Figure 5.6(a) shows a 2d plot of the reconstructed 3d tomography of a printed porous SnO_2 film after calcination. The interconnected porous SnO_2 network is clearly visible as well as the intercon-

nected pores. To ensure a good percolation between the pores a skeletonization is performed using the software Amira 5.6 (FEI Company), where the pore volume is reduced to a medial axis of the pore (see Figure 5.6(b)). The resulting network represents a skeleton of the pore-system and shows the interconnection of the pores. This results in a center-line tree picture, which shows a very tight connection of the pores, which should enable a complete infiltration of CSPE-1(lq) into the semiconductor network.

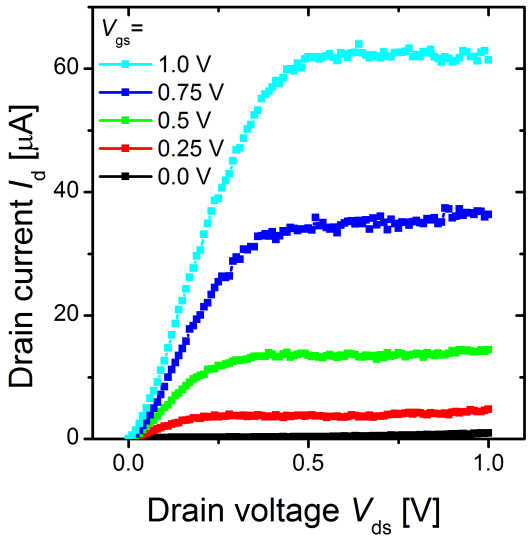
With this thorough analysis of the porous SnO_2 semiconductor network, CSPE-1(lq) is infiltrated into a vertical channel EG-FET for further analysis of its performance as channel material.

5.3 Vertical Channel EG-FET

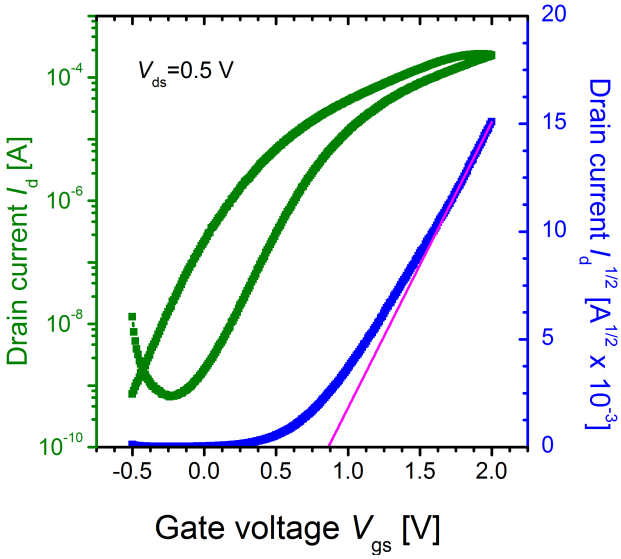
In the upcoming section the porous SnO_2 is used in vertical channel field-effect transistors and the prepared devices are electrically characterized with respect to geometrical variations. The characteristic device parameters are extracted and compared to a simulated system provided by project partners [87]. The channel is prepared by inkjet printing of two successive layers of SnO_2 precursor solution onto the source electrode of width W_{source}. The resulting film thickness, which corresponds to the channel length L amounts to 45 nm. Two layer printing is found necessary to ensure sufficient thickness to avoid electrical short-circuits between source and drain, where latter is, like the source electrode, fabricated by means of lithographic lift-off technique. By applying two layers of SnO_2 precursor, possible cracks in the first layer are filled up and the overall film quality is improved. The width of the drain electrode is chosen in all cases to be equal to the source electrode width $W_{\text{drain}} = W_{\text{source}}$. To get a better understanding of the electrode geometry, Figure 5.8 is shown, which is later used for the calculation of the channel width and the areal capacitance of the semiconductor/CSPE interface in the v-FET. In order to find the geometry for the best performing v-FET, four different electrode widths are tested. The electrodes define the channel geometry, because source and drain electrodes cross each other perpendicularly and the overlap of source and drain electrode defines the quadratic channel area. Different electrodes are prepared with widths of 0.25 µm, 0.5 µm, 1 µm and 2 µm. This way electrode areas as indicated in Figure 5.9 of $6.25 \cdot 10^{-2}\,\mu\text{m}^2$, $0.25\,\mu\text{m}^2$, $1\,\mu\text{m}^2$ and $4\,\mu\text{m}^2$ are established. Transfer and output curves of all four representative devices are presented in Figure 5.7. The analysis is performed, as described in section 3.1.8. In the porous semiconductor of the v-FET, the geometrical channel width W_{channel} is not clearly defined. Therefore, it is necessary to use a model, which approximates the complex porous structure. In the present thesis, the porous channel volume is replaced by semiconducting pillars extending from source to drain electrode. The remainder of the bulk volume is initially filled with air and later with CSPE-1(sd) (see Figure 5.8). The SnO_2 to bulk ratio is determined from the analysis of the electron tomography and turned out to be η =51.7 %, where the bulk volume V_{bulk} is taken as the entire volume spanned between the crossing part of source and drain electrode.


V_{ds}=0.5 V
Drain current I_d [A]
Drain current $I_d^{1/2}$ [$A^{1/2}$ x 10^{-3}]
Gate voltage V_{gs} [V]

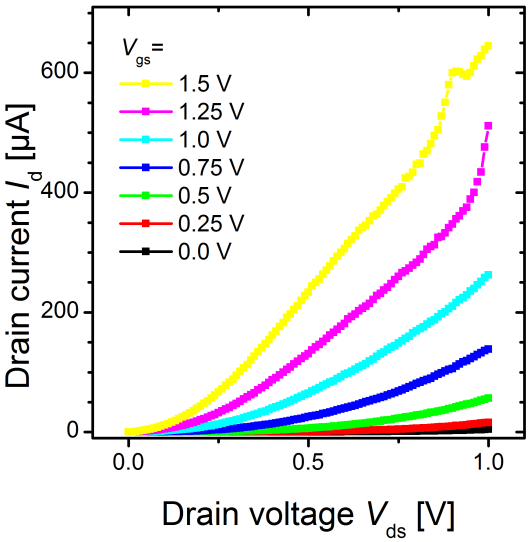
(a)


V_{gs}=
1.0 V
0.75 V
0.5 V
0.25 V
0.0 V
Drain current I_d [μA]
Drain voltage V_{ds} [V]

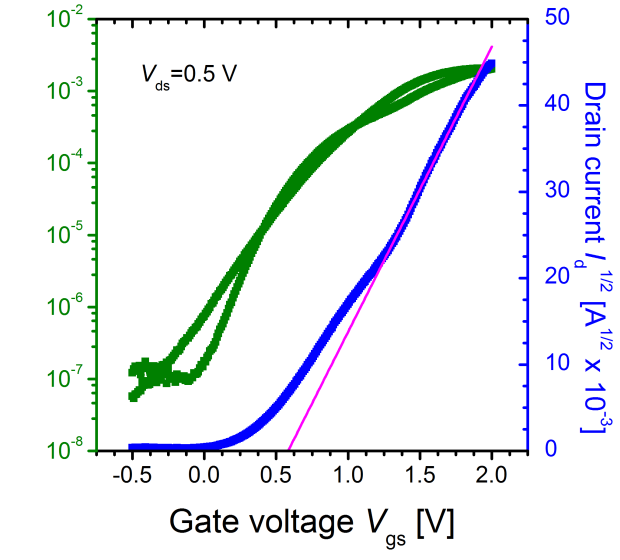
(b)


V_{ds}=0.5 V
Drain current I_d [A]
Drain current $I_d^{1/2}$ [$A^{1/2}$ x 10^{-3}]
Gate voltage V_{gs} [V]

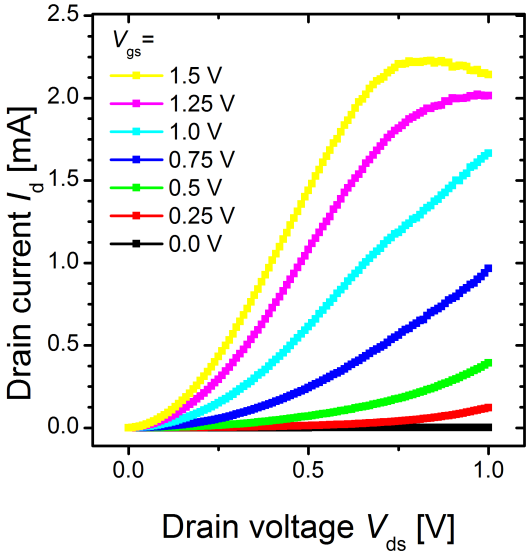
(c)


V_{gs}=
1.5 V
1.25 V
1.0 V
0.75 V
0.5 V
0.25 V
0.0 V
Drain current I_d [μA]
Drain voltage V_{ds} [V]

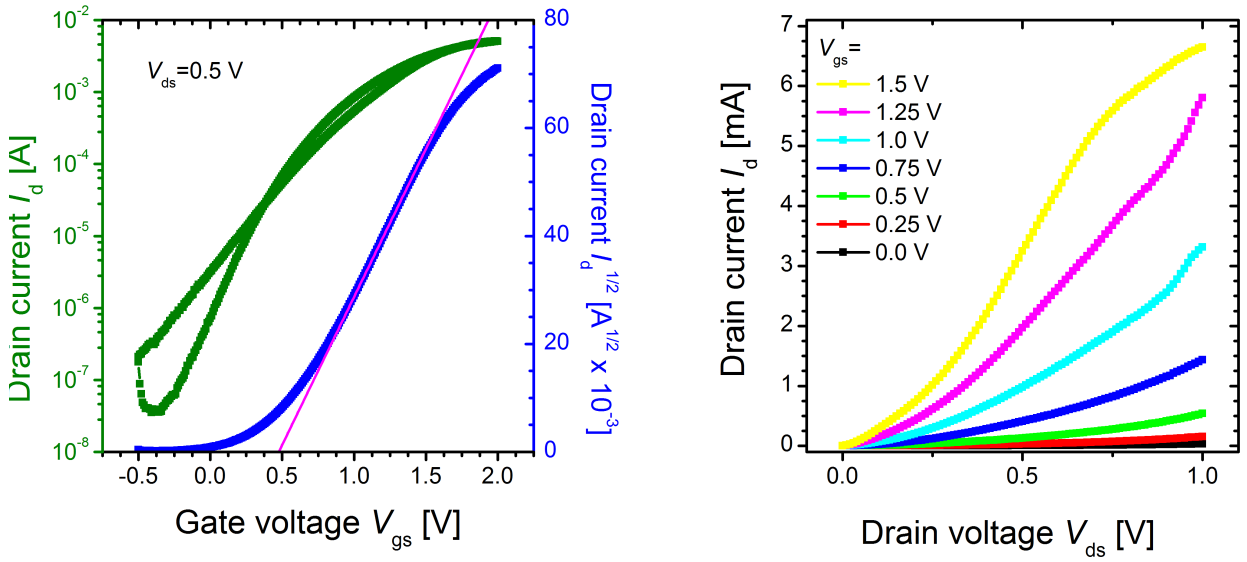
(d)


V_{ds}=0.5 V
Drain current I_d [A]
Drain current $I_d^{1/2}$ [$A^{1/2}$ x 10^{-3}]
Gate voltage V_{gs} [V]

(e)


V_{gs}=
1.5 V
1.25 V
1.0 V
0.75 V
0.5 V
0.25 V
0.0 V
Drain current I_d [mA]
Drain voltage V_{ds} [V]

(f)



(g) (h)

Figure 5.7.: Transfer and output curves of four v-FETs with different electrode areas: (a) and (b) 0.0625 μm^2, (c) and (d) 0.25 μm^2, (e) and (f) 1 μm^2 and (g) and (h) 4 μm^2. For each device the graph on the left side represents the transfer characteristic curve (green) and the $I_d{}^{1/2}$ characteristic curve (blue). The graph on the right side displays the output characteristics with V_{gs} varying from 0.0 V to 1.5 V in steps of 0.25 V.

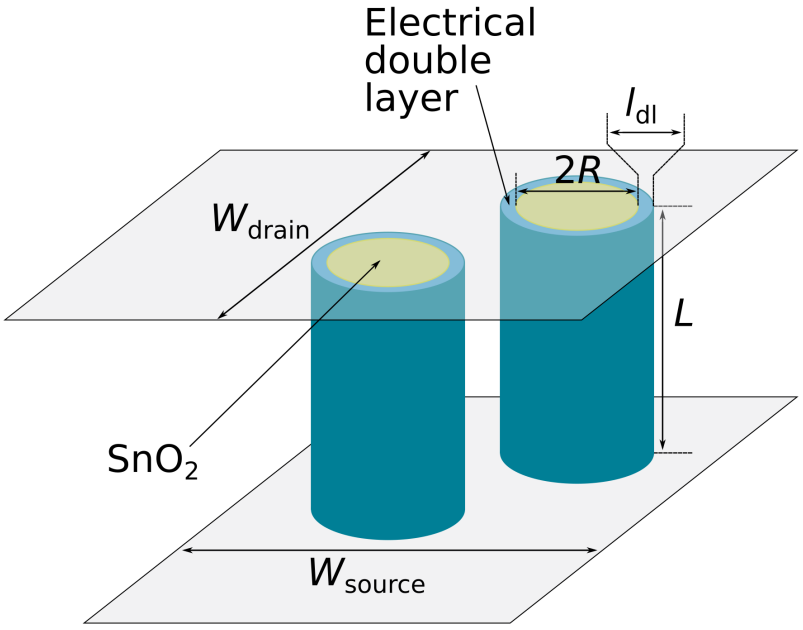


Figure 5.8.: Schematic of the v-FET model where pillars are replacing the porous semiconductor. The dimensions are indicated in the figure using R as pillar radius, L as pillar/channel length and W_{source} and W_{drain} as the electrode widths.

The radius of the pillars R is taken as half of the width of the SnO_2 filaments and amounts to 10 nm. With these values the number of pillars N_{pillars} can be calculated. It yields:

$$V_{\text{SnO2}} = V_{\text{bulk}} \cdot \eta \tag{5.1}$$
$$= \pi \cdot R^2 \cdot L \cdot N_{\text{pillars}} \tag{5.2}$$

this results in

$$N_{\text{pillars}} = \frac{V_{\text{bulk}} \cdot \eta}{\pi \cdot R^2 \cdot L} \tag{5.3}$$

with V_{bulk} the bulk volume ($250 \cdot 250 \cdot 45\,\text{nm}^3$), V_{SnO_2} the volume of the solid SnO_2 network, R the pillar radius and L the channel length (45 nm). With the resulting number of pillars $N_{\text{pillars}} = 103$ the total width of the transistor channel can be calculated. It yields

$$W_{\text{channel}} = N_{\text{pillars}} \cdot 2\pi R, \tag{5.4}$$

this results in a channel width $W_{\text{channel}} = 6.5\,\mu\text{m}$. The areal double layer capacitance is then calculated following the route of Roddaro et al. [88]. They determined the capacitance C'_{dl} and the areal capacitance C_{dl} for a cylindrical capacitor using the equations

$$C'_{\text{dl}} = \frac{2\pi\epsilon_0\epsilon_{\text{r}}L}{\ln\left(1+\frac{l_{\text{dl}}}{R}\right)} \text{ or} \tag{5.5}$$
$$C_{\text{dl}} = \frac{\epsilon_0\epsilon_{\text{r}}}{\ln\left(1+\frac{l_{\text{dl}}}{R}\right)R} \tag{5.6}$$

with ϵ_0 the permittivity of free space, ϵ_{r} the relative permittivity of CSPE-1(sd) and l_{dl} the thickness of the electric double layer, which can be assumed to be $\sim$2 nm for highly concentrated electrolyte solutions [89–91]. According to Dzhavakhidze et al. [92] the relative permittivity of an electrical double layer close to a solid charged interface reduces to $\epsilon_{\text{r}} = 4$. This value for the dielectric constant was found to be independent of the actual permittivity values of the utilized bulk materials. The value for the electrical areal double layer capacitance then results to $C_{\text{dl}} = 1.94\,\mu\text{F cm}^{-2}$. With the values for channel width and areal double layer capacitance, the v-FETs can be analyzed as discussed in section 3.1.8 and the obtained results are displayed in table 5.1.

A variation of the electrode area $\Gamma = W_{\text{source}} \times W_{\text{drain}}$ as marked in red in Figure 5.9 should in an ideal v-FET only change the on- and off-currents of the transistor. This can be understood by

the proportional increase of the number of pillars connecting the source and drain electrodes. This increased number of the pillars implies a proportionally increasing total width of the transistor channel W_{channel}. Since the width of a field-effect transistor is directly proportional to the drain current I_{d} (see eq. (2.10)) this explains the expected behavior that both, the on- and off-currents should increase proportionally to the electrode area Γ. Doubling the electrode width results in a fourfold electrode area, which translates into a fourfold channel width and therefore to a fourfold drain current.

Table 5.1.: On-current ($I_{\text{d,on}}$), off-current ($I_{\text{d,off}}$), on/off-current ratio (on/off-current ratio), subthreshold swing (SS), threshold voltage (V_{th}), field-effect mobility (μ_{FET}) and current density j'_{d} for v-FETs with four different electrode areas.

electrode width [μm]	electrode area [μm^2]	$I_{\text{d,on}}$ [mA]	$I_{\text{d,off}}$ [nA]	on/off-current ratio [a.u.]	SS [$\frac{mV}{dec}$]	V_{th} [V]	μ_{FET} [$\frac{cm^2}{Vs}$]	j'_{d} [$\frac{MA}{cm}$]
0.25	$6.25{\cdot}10^{-2}$	0.206	0.004	10^8	141	0.65	2.22	0.33
0.5	0.25	0.232	0.72	10^6	193	0.86	0.62	0.09
1	1	2.01	57	10^5	342	0.58	1.35	0.22
2	4	5.08	40	10^5	405	0.48	0.86	0.12

As a consequence the on- and off-current **densities** j'_{d} of devices with different electrode areas should stay constant, independent of the utilized electrode area. However, the experimentally observed drain currents do not follow this expected increase. The observed I_{d} currents increase with respect to the device with $W_{\text{source}} = 0.25\,\mu$m, from now on referred to as $0.25\,\mu$m-device, by the geometrical factors 1.1 (4) for the $0.5\,\mu$m-device, 10.7 (16) for the $1\,\mu$m-device, and 24 (64) for the $2\,\mu$m-device where the numbers in brackets are the theoretically expected factors. The on-current densities j'_{d} shown in table 5.1 also drop for larger electrode areas. To explain this discrepancy further considerations are necessary. Two reasons are identified so far to explain the deviation in the on-current densities j'_{d} between expected and measured values. These reasons are:

- the influence of stray currents for an purposely introduced electrode overhang and
- an incomplete penetration of the CSPE-1(lq) with the narrow gap between the two metallic electrodes into the porous semiconductor leaving the inner part of the FET without gating effect.

The influence of stray currents is expected due to a purposely introduced 100 nm overhang of the source electrode over the drain electrode marked in green in Figure 5.9(b) and an equivalent overhang of the drain electrode over the source electrode in the other direction marked in orange.

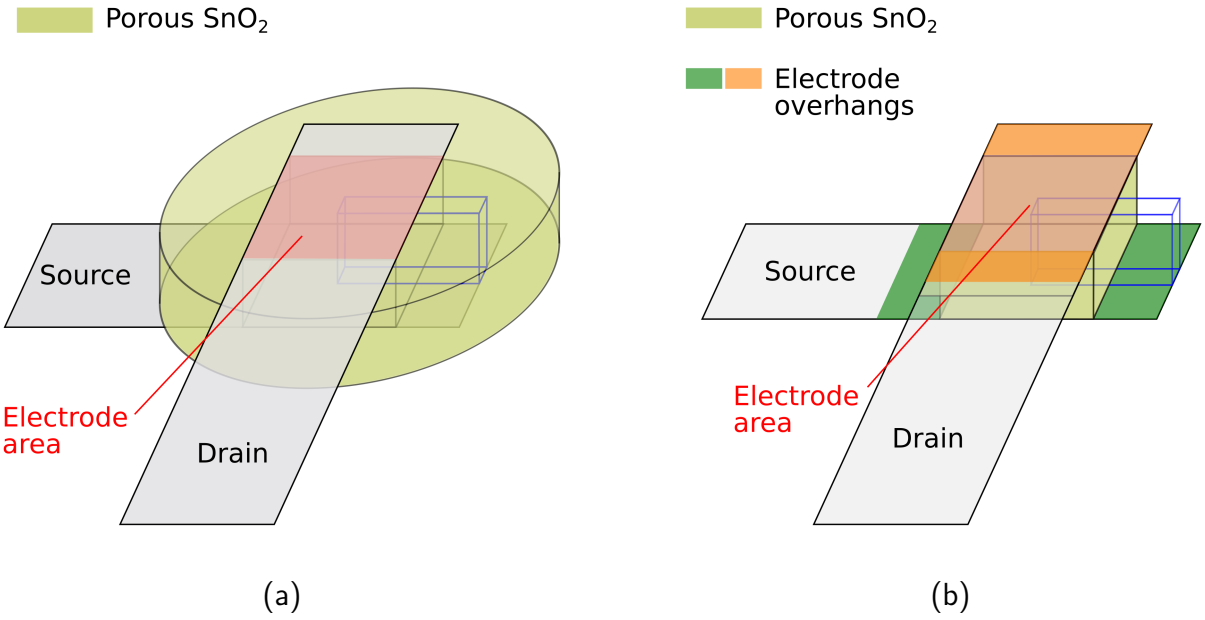


Figure 5.9.: Schematic of the overhang of source and drain electrode displayed with (a) a drop shaped semiconductor and (b) a cuboid shaped semiconductor.

This overhang is introduced to ensure that the magnitude of the electrode area $\Gamma = W_{\text{source}} \cdot W_{\text{drain}}$ throughout the lithographic process stays constant despite possible deviations from the intended position of the electrodes by lithographic inaccuracies. Thereby, stray currents flow from the edges of the drain electrode through the semiconductor outside of the electrode area to the overhanging source electrode. The electrons follow the electric stray field, which results from an applied voltage between source and drain at the edges of the electrodes. The effect is vice versa for the reverse electrode arrangement. In order to simulate the magnitude of the stray currents, the channel at the edge of the electrode area is described by a semiconductor cuboid (200 nm × 50 nm × 20 nm) as indicated exemplarily by the cuboid with the blue lines in Figure 5.9(a), which displays a complete overlap of the source electrode with the semiconductor but only half with the drain electrode as displayed in Figure 5.10(a). This cuboid thereby represents a single semiconducting filament of width $W = 20\,\text{nm}$ and lateral extension of 200 nm ranging uniformly from source to drain with a channel length $L = 50\,\text{nm}$. These cuboids are arranged in parallel and are separated by the pores, which are filled with the electrolyte being responsible for the gating effect. The cuboid is connected laterally to a gate dielectric and a gate electrode, which simulates the CSPE-1(sd) properties with applied gate voltage. The resulting electric fields and the electric currents are simulated using a drift-diffusion model utilizing COMSOL 5.1. The actual calculations were performed in collaboration with project partners [87]. For determining the ratio between the current flowing through the electrode area and the current through the region outside the electrode area, the following calculations are performed: First, the current I_{tot} through the semiconductor cuboid in Figure 5.10(a) is calculated. Then the current I^*_{ref} through a cuboid as

shown in Figure 5.10(b) is calculated as an ideal reference system. From these two calculations, one can determine the stray current I^*_{stray} for a single filament at the edge of the electrode area. It yields: $I^*_{\text{stray}} = I_{\text{tot}} - I^*_{\text{ref}}$.

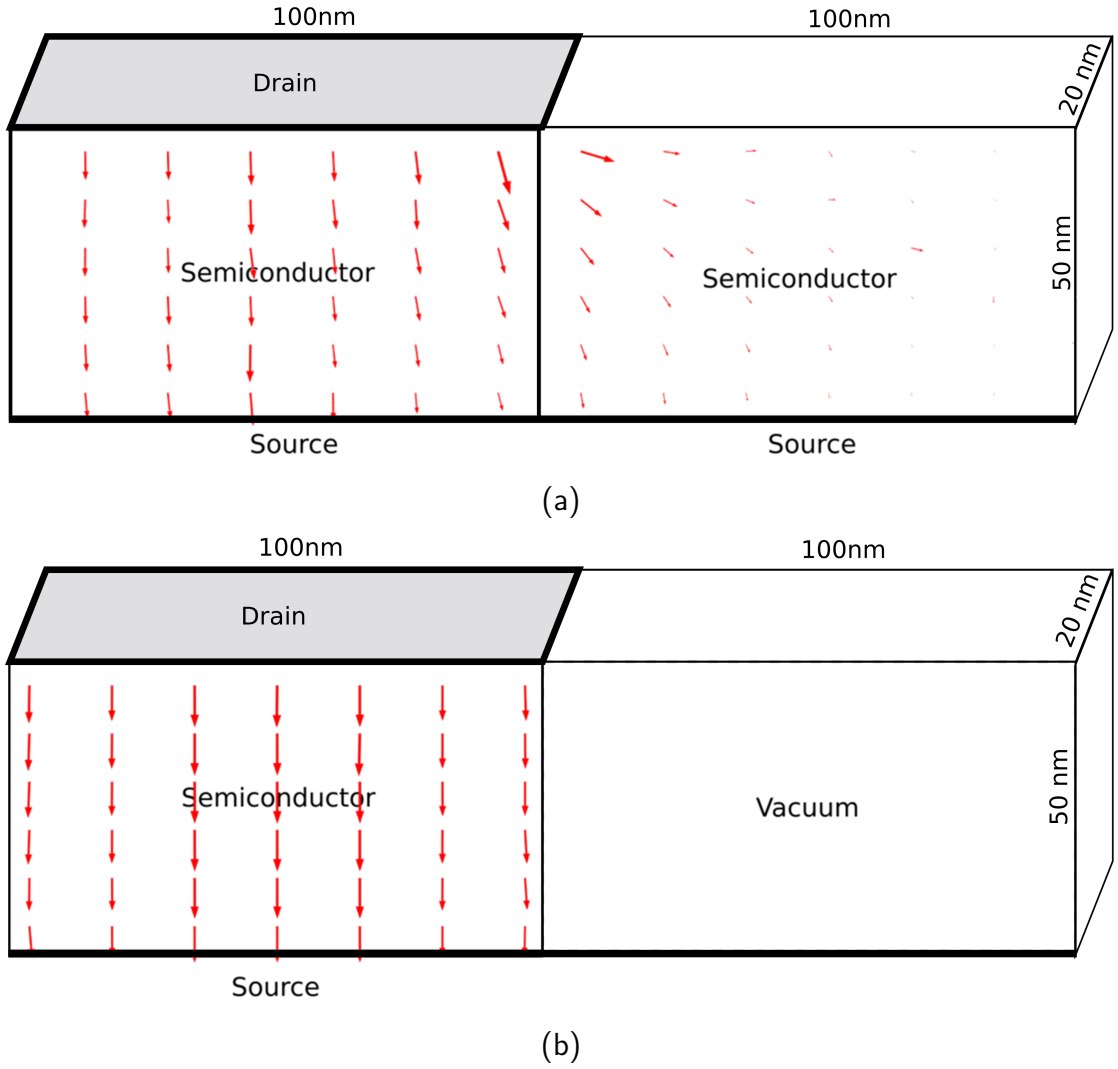


Figure 5.10.: (a) Schematic drawing of a single semiconductor filament at the edge of the channel area with the current density indicated by red arrows and (b) a schematic plot of an ideal channel edge without overhanging semiconductor material for comparison.

In the following the ratio of this stray current to the reference current is calculated to estimate its influence on the different experimental geometries.

Using I^*_{stray} and I^*_{ref} the currents for the actual devices can be calculated as follows:

$$I_{\text{stray}} = 4 \cdot W_{\text{source}} \cdot \frac{I^*_{\text{stray}}}{20\,\text{nm}} \cdot k \cdot \eta \quad \text{and} \tag{5.7}$$

$$I_{\text{ref}} = \Gamma \cdot \frac{I^*_{\text{ref}}}{20\,\text{nm} \cdot 100\,\text{nm}} \cdot \eta \tag{5.8}$$

where the stray current I^*_{stray} obtained by computer simulation is normalized to the filament width (20 nm) and resized to the channel circumference of the electrode area ($4{\cdot}W_{\text{source}}$). This can be done because the stray currents from drain to source and from source to drain are equal. Multiplication with η considers the porosity of the channel material and multiplication with k takes into account that not every ligament is crossed perpendicularly by the source/drain electrode edges, which results in a larger effective filament and pore width. To determine k, a line of the same length as the electrode width W_{source} is randomly drawn through an SEM micrograph of the porous semiconductor and the filament/pore interfaces are counted. Utilizing a 250 nm line, an average of 7 of these interfaces is crossed instead of 12.5, as assumed in the model calculation. The correction factor k results in $k \approx 0.56$. For the reference current the value I^*_{ref} obtained from computer simulation is normalized to the 100 nm × 20 nm electrode area of the cuboid. This normalized value is then multiplied with Γ to account for the experimentally utilized electrode area. Again η makes up for the porosity of the semiconductor. With the knowledge of the currents I_{ref} and I_{stray} the ratio r between the current through and next to the electrode area can be calculated by

$$r = \frac{I_{\text{stray}}}{I_{\text{ref}}} = \frac{4 \cdot \sqrt{\Gamma} \cdot \dfrac{I^*_{\text{stray}}}{20\,\text{nm}} \cdot k \cdot \eta}{\Gamma \cdot \dfrac{I^*_{\text{ref}}}{20\,\text{nm} \cdot 100\,\text{nm}} \cdot \eta}. \tag{5.9}$$

The ratio of the stray current to the reference current is plotted as a function of electrode area in Figure 5.11.

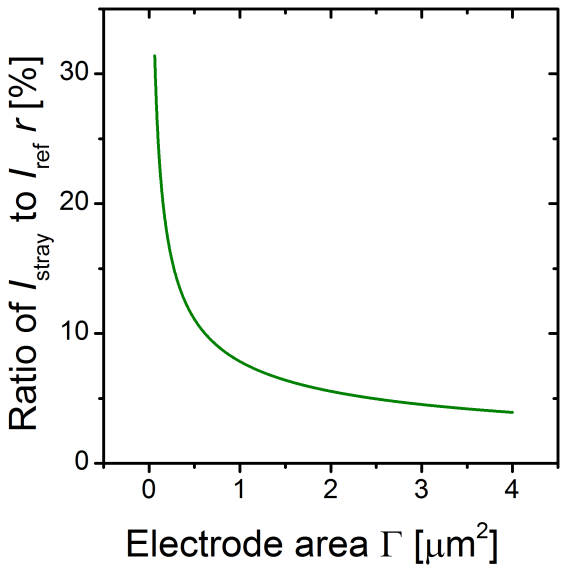


Figure 5.11.: Ratio of the stray current I_{stray} to the reference current I_{ref} in % as a function of the electrode area Γ.

From Figure 5.11 it can be seen that the ratio of stray current becomes large, when the electrode areas get small. The drain (on-)currents flowing through the electrode areas for the different geometries can then be calculated to $I_\mathrm{d}(0.0625) = 0.142\,\mathrm{mA}$, $I_\mathrm{d}(0.25) = 0.195\,\mathrm{mA}$, $I_\mathrm{d}(1) = 1.85\,\mathrm{mA}$ and $I_\mathrm{d}(4) = 4.88\,\mathrm{mA}$, respectively. This corresponds to geometrical factors of 1.37 (4), 13 (16) and 34 (64) with respect to $I_\mathrm{d}(0.0625)$ for the on-currents of larger electrode areas. Again the values in the brackets are the expected factors. This correction reduces the discrepancies between the expected current values for I_d and the measured values for the respective electrode areas but still does not explain the deviation satisfactorily.

Therefore, the second hypothesis for the discrepancy between expected and measured values of the on-currents I_d or equivalently the decreasing current densities j'_d for the devices with increasing electrode size, namely a finite penetration depth of the printed CSPE-1(lq) into the SnO_2 network is investigated. The rationale behind this model is that CSPE-1(lq) has to penetrate into the active volume of the semiconductor in between source and drain from the sides since the electrodes are continuous and impenetrable due to the fabrication process (see section 3.3.7). The penetration depth is thereby limited, since the enclosed air in the pores in between the electrodes has only limited possibility to escape once the liquid electrolyte is applied. In the present description of the influence of the limited penetration depth on I_d, it is assumed that the liquid penetrates from all four edges by the same length W_CSPE as shown in Figure 5.12. In order to determine the influence on the current density j'_d, the amount of the electrode area, which is not filled with CSPE-1(sd), has to be described.

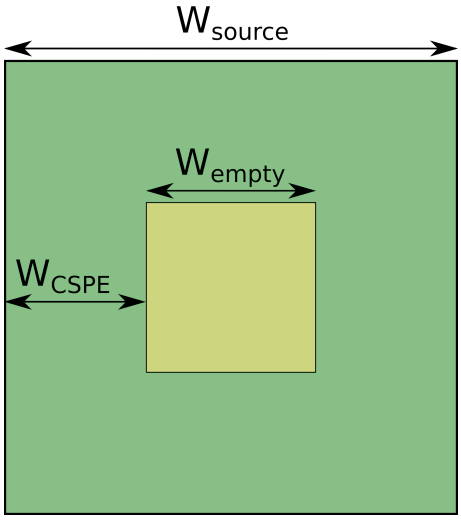


Figure 5.12.: Geometrical consideration of the penetration depth of CSPE-1(lq) into the channel area.

A good measure for the penetration depth W_CSPE can be derived from the measured on-current densities for the different electrode sizes. The on-current density thereby can be seen as the theoretically expected constant current density $j'_{\mathrm{d},0.25}$ (for the device with electrode width 0.25 μm) in the CSPE-1(sd) penetrated area and in the non-penetrated area the current density is assumed

to be zero. The averaged current density over the complete electrode area thereby resembles the measured on-current density $j'_{\mathrm{d},0.5/1/2}$. With the dimensions shown in Figure 5.12 it yields:

$$j'_{\mathrm{d},0.5/1/2} = \frac{(W^2_{\mathrm{source}} - W^2_{\mathrm{empty}}) \cdot j'_{\mathrm{d},0.25}}{W^2_{\mathrm{source}}} \tag{5.10}$$

where W_{empty} is the length of the not CSPE-1(sd) filled square as seen in Figure 5.12 and $j'_{\mathrm{d},0.25/0.5/1/2}$ the experimentally determined current densities of the respective devices. In this consideration the 0.25 μm-device is assumed to be fully penetrated by CSPE-1(sd). From eq. (5.10) the penetration depth W_{CSPE} for each geometry can be calculated using $W_{\mathrm{CSPE}} = \frac{W_{\mathrm{source}} - W_{\mathrm{empty}}}{2}$ and results in

$$W_{\mathrm{empty}} = W_{\mathrm{source}} \cdot \sqrt{1 - \frac{j'_{\mathrm{d},0.5/1/2}}{j'_{\mathrm{d},0.25}}} \quad \text{and} \tag{5.11}$$

$$W_{\mathrm{CSPE},0.5/1/2} = \frac{W_{\mathrm{source}}}{2} \cdot \left(1 - \sqrt{1 - \frac{j'_{\mathrm{d},0.5/1/2}}{j'_{\mathrm{d},0.25}}}\right) \tag{5.12}$$

Equation 5.12 yields the penetration depth from the edges of the electrodes of 47 nm for the 0.5 μm-device, 0.276 μm for the 1 μm-device and 0.307 μm for the 2 μm-device. The penetration depth of ~0.3 μm for the 1 μm- and the 2 μm-device is self-consistent with the assumption of a fully penetrated 0.25 μm-device. The 0.5 μm-device is not delivering a consistent result and seems to suffer from further problems, preventing CSPE-1(lq) from infiltrating. At the same time, the limited penetration depth with 1 μm and 2 μm electrode width explains the deviation from the expected on-currents for these device geometries satisfactorily.

With the knowledge of the penetration depths, the field-effect mobilities of the devices can be recalculated. Substituting the channel area Γ with the actually CSPE-1(sd) gated area $W^2_{\mathrm{source}} - W^2_{\mathrm{empty}}$ in the channel volume in eq. (5.1) and with the new effective channel width the effective field-effect mobilities for the larger electrode area devices result in $\mu_{\mathrm{FET},0.5} = 1.82\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$, $\mu_{\mathrm{FET},1} = 1.69\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ and $\mu_{\mathrm{FET},2} = 1.67\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$. These values agree with the mobility value of the 0.25 μm device quite well. Still, these are rather small mobility values compared to the intrinsic mobility of $\mu_0 = 250\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ of SnO_2 [93] and μ_{FET} values of SnO_2 single crystal nanowires of $207\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ [59]. It seems that in case of the printed porous SnO_2, its nanocrystalline nature reduces the mobility considerably. For a channel length of 45 nm and a crystal size of 3-5 nm, as shown in the TEM micrograph in Figure 5.4(a), the electrons have to pass more than 8 grain boundaries, which can easily be the reason for the small values of μ_{FET}.

The full potential of the device, however, can be seen if the current density per unit area is considered. For the four geometries the effective current densities $j_{\mathrm{d,effective}}$ are found to be $0.33\,\mathrm{MA\,cm^{-2}}$ for the 0.25 μm-device, $0.27\,\mathrm{MA\,cm^{-2}}$ for the 0.5 μm-device, $0.25\,\mathrm{MA\,cm^{-2}}$ for the

1 μm-device and 0.25 MA cm^{-2} for the 2 μm-device. Compared to the current density from table 5.1, calculated with the electrode areas Γ of the respective devices, the effective current densities $j_{\mathrm{d,effective}}$ are calculated with the effective electrode areas $W^2_{\mathrm{source}} - W^2_{\mathrm{empty}}$. The values then match the current density for the 0.25 μm-device, which is assumed to be fully CSPE-1(sd) penetrated, satisfactorily. Such high current densities, which are almost 2 orders of magnitude higher than all reported values of current densities of printed materials up to now [67, 94], can be explained by the favorable geometry and the large channel width of the porous SnO_2 semiconductor network. As a result of the CSPE gating technique the equivalent of more than 100 pillars/fibers can be switched simultaneously using a single gate potential. Despite the very large current density the electrical characteristic curves of the 0.25 μm-device are close to ideal. The output curves exhibit the classical ${V_{\mathrm{gs}}}^2$ behavior and a clear current saturation for $V_{\mathrm{ds}} > V_{\mathrm{gs}}$ (see Figure 5.7).

The output characteristics of the devices with larger electrode areas as displayed in figures 5.7(f) and (h) are not ideal. The I_{d} characteristics of the 0.5 μm-device in Figure 5.7(d) are not discussed since the current densities observed for this device are atypical and seem to result from unknown device defects. For the other devices one observes an initial S-shape of the I_{d} characteristics combined with a shift of I_{d} characteristics to higher V_{ds} values. In addition, the drain currents do not completely saturate anymore. The S-shape of the output characteristics can be reasoned to be a consequence of the finite penetration depth of the electrolyte into the channel region. Such a finite penetration depth most probably results in a non-uniform forefront of the CSPE-1(lq). This is due to the irregular semiconductor network or to remainders of pyrolytic carbon in the pores due to an oxygen deficiency during the calcination process. This effect has to be discussed. Therefore, a simple example for such a non-uniform distribution is shown in Figure 5.13. In this case the center of the semiconductor layer is penetrated easier and the edges fill up later or stay empty dependent on the trapped air in the pores. In this shape the forefront of the CSPE-1(lq) solidifies.

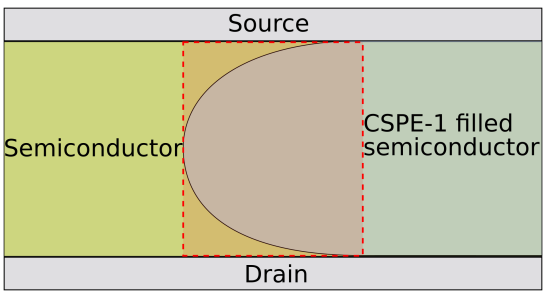


Figure 5.13.: Schematics of a cross section of the filling of the CSPE-1(sd) in the porous SnO_2 network in between source and drain electrode indicating an inhomogeneous filling with CSPE-1(sd) at the limit of the penetration depth.

To discuss the consequences, a red frame and shading is added in Figure 5.13 to mark the location, where the channel is not filled uniformly anymore over the whole channel length L. In this exemplary case the electrolyte is missing near the electrodes and no gating effect occurs in these regions. Independent of the shape of the forefront the consequences of a partial gating effect is similar for different shapes. Under an applied gate voltage the channel will only form in the CSPE-1(sd) filled regions. The non-gated regions next to the electrodes will result in large contact barriers. It was shown that such contact barriers lead to the observed S-shape of the output characteristics [95] as observed experimentally in the present study. This phenomenon of an incomplete channel formation is present all along the inner edges of the non-gated part of the semiconductor. In addition, there may be at some filaments an injection barrier between the metal electrodes and the SnO_2 filaments. The origin of these injection barriers can be seen in the fabrication step of depositing the metal electrode on the dried precursor ink before calcination. This means that some of the filaments are not connected to the drain electrode directly since they are covered by a thin polymer layer before metalization, which after calcination forms an air gap or a layer of pyrolytic carbon, which is equivalent to a potential barrier. Such an intermediate layer between drain and channel would act as an injection barrier leading to the S-shaped onset of the output characteristic, as well. As discussed before one would also expect that the off-currents scale with the electrode area Γ. The experimental off-currents t[87]aken from the minimum of the transfer characteristics of the larger FET devices from figures 5.7(c), (e) and (g), increase, however, by 4 orders of magnitude instead of the factor of 64 as expected. This unexpected increase can also be explained by the finite penetration depth of the electrolyte. It is found, that the semiconductor without electrolyte gating has a higher conductivity than the CSPE-1(sd) filled semiconductor with electrolyte gating. Thus, the non-gated semiconductor volume shows higher currents than the gated regions of the fully CSPE-1(sd) filled fraction of the active channel volume. This can be understood by examining the energetics of the device in the off state of a gated and a non-gated filament. The electrolyte gating is performed between SnO_2 and platinum. In order to equalize the Fermi levels of SnO_2 located at -4.9 eV [96] and of platinum located at about -5.65 eV [97] electrons have to flow from SnO_2 towards platinum. In the case of an electrolyte in contact with SnO_2 and platinum the ions form electrical double layers as compensation at the respective interfaces. This results in the extraction of electrons from the SnO_2 and thus lowers the conductivity of the channel. In the empty channel region this is not the case and the conductivity is consequently higher. With a large fraction of non-gated semiconductor in the electrode area the off-current is dominated by the conductivity of the pure semiconductor and increases strongly with growing electrode size. The varying threshold voltages V_{th} and the change in the subthreshold swing SS are not understood in the present case but may be related to the trap density at the electrolyte/semiconductor interface, which is difficult to address experimentally.

After the thorough analysis of the v-FET characteristic values, a brief analysis of the time constants τ_{RC} and τ_{transit} are performed. To calculate τ_{RC}, the electrolyte resistance and the

capacitance are calculated. With an average gate-to-channel distance d of 50 μm, a thickness of CSPE-1(sd) of 1 μm, the electrolyte width of 250 nm, corresponding to the channel width yielding in A and the ionic conductivity of the CSPE-1(sd) at room temperature σ_{el}(=5.37$\cdot$ 10^{-3} S/cm) the resistance R_{el} can be calculated. From eq. (2.15) the resistance results in $R_{elec,v\text{-}FET} = 3.7{\cdot}10^{8}\,\Omega$. The areal capacitance is calculated from eq. (5.6) and results in $C_{dl} = 1.94\,\mu F\,cm^{-2}$. With a channel width $W_{channel} = 6.5\,\mu$m and the channel length $L = 45$ nm the capacitance is calculated to be $C'_{dl,v\text{-}FET} = 178$ pF. The time constant of the RC-circuit results in $\tau_{RC} = R_{elec,v\text{-}FET} \cdot C'_{dl,v\text{-}FET} = 2.1\,\mu$s. Anyhow, the actual capacitance has to be calculated for the much larger surface of the entire printed droplet. The droplet has a diameter of $\sim$50 μm which results in a surface area, which is about 10000 times larger than the channel surface in the electrode area. This increases the time constant to $\tau_{RC} = 21$ ms. The transit time of the electrons in the SnO_2 network can be calculated from eq. (2.11). Taking the channel length of 45 nm, the field-effect mobility of 2.2 $cm^2\,V^{-1}\,s^{-1}$ and the drain voltage of 0.5 V the transit time can then be calculated to $\tau_{transit} = 18.4$ ps. The actual device switching speed is thus limited by the large electrolyte resistance and the large semiconductor surface, due to the printed droplet. This problem will be dealt with in the next section 5.4.

To gain further insight into the material and the v-FET performance, simulations were performed to support the measured data and give further insight into the functionality of the porous channel material. The simulations have been conducted in the group of Professor Wenzel and are also used to find parameters to optimize the channel material for future applications [87]. Using drift-diffusion calculations, the charge density distributions for different morphologies (see appendix G) are calculated. The electrolyte is thereby replaced by a dielectric with a thickness of 2 nm and a relative permittivity of 4, as introduced earlier. The work function of the gate metal Pt is set to -5.95 eV, where experimental values from literature of -5.65 eV are reported [97]. The work function of SnO_2 is set to -4.9 eV [96] and the band gap to 3.6 eV. Source and drain electrode are connected to the semiconductor assuming ohmic contacts. The carrier concentration of SnO_2 is considered to be 5.4$\cdot$ 10^{18} cm^{-3} which is at the higher end of previously reported values [98, 99]. The electron mobility is set to 3.0 $cm^2\,V^{-1}\,s^{-1}$, which is at the lower end of reported values [99] and matches the μ_{FET} of 2.2 $cm^2\,V^{-1}\,s^{-1}$ shown in table 5.1. Experimentally determined values for polycrystalline SnO_2 films show mobilities in the range of 10-20 $cm^2\,V^{-1}\,s^{-1}$ for compact films with crystallite sizes of 10-30 nm. In this case the porous structure and the crystallite sizes of 3-5 nm can cause the deviations from literature values. With these boundary conditions transfer curves are simulated with a drain voltage V_{ds} of 0.5 V in a voltage range between V_{gs}=0.0 V and 2 V. For $V_{gs} < 0.0$ V the leakage current, which is not taken into account in the calculations dominates the drain current. Figure 5.14 shows simulated transfer curves for different semiconductor morphologies (see Figure 5.14(a)) and different carrier concentrations (see Figure 5.14(b)). Figure 5.14(a) shows, that with a changed morphology towards smaller pore sizes and filament widths the drain current can be increased and at the same time the on/off-current ratio increases. A channel

with smaller pore sizes and filament widths would thus offer an even higher current density. The carrier concentration is, however, in an optimal region.

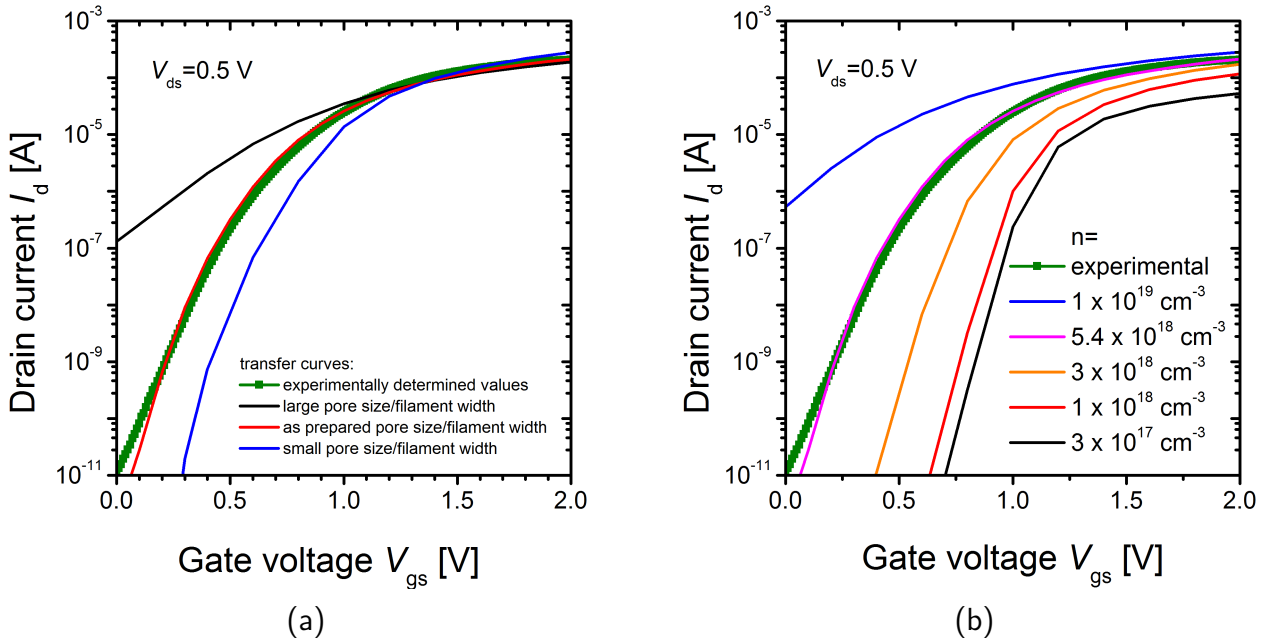


Figure 5.14.: Comparison of the experimental (0.25 μm) and theoretical transfer curves: (a) the theoretical curves are calculated from the drift diffusion model using fixed parameters for the work function Ψ, the relative permittivity ϵ_r, the field-effect mobility μ_{FET} and the carrier concentration n for three different morphologies (see appendix G.1). (b) Influence of different carrier concentrations on the transfer curves determined using otherwise the same parameters as for Figure (a) utilizing the experimental morphology taken from an SEM micrograph (see appendix G.1(b)). The green curve in both figures resembles the experimental transfer characteristic.

With an optimization towards smaller pores and smaller semiconductor filament widths, the problem of crosstalk between opposing pore walls may appear due to an overlap of the two Gouy-Chapman layers in the electrolyte and due to an overlap of the two space charge regimes forming on both sides of the same semiconductor filament. This may lead to shielding effects in the center of the electrode area. To check on these concerns, simulations on the extension of the channel inside the semiconductor filament were performed, which is calculated to ~1 nm. Therefore the filament width could be further reduced to optimize the performance of the transistor. The thickness of the electric double layer in the CSPE-1(sd) is assumed from literature where Bourgh et al. used an extended Poisson-Boltzmann model and found the dimension of the electric double layer to reach ~1.5 nm [100] into an electrolyte. Assuming this electric double layer thickness the pores could also be reduced to about 3 times this size which amounts to ~4.5 nm. These results give rise to the assumption, that smaller pores and filaments could actually improve the performance of the v-FET without compromising the channel formation in the porous semiconductor network.

Still the functionality and penetration of the CSPE-1(lq) into such porous semiconductors with reduced channel width has to be guaranteed.

5.4 Reduction of Switching Speed

To address the question of achieving a low value for τ_{RC}, one has to overcome the problem of large gate-to-channel distances for displaced gates. Therefore a novel approach for an EG-FET with a back-gate geometry is presented. As gate electrode ITO is used, covered with porous Al_2O_3 to define a spatial separation between channel and gate. Porous SnO_2 as semiconductor and platinum as source and drain electrodes are applied subsequently. The resulting device geometry is shown in Figure 5.15(a). Electron beam lithography is used to structure and locate the electrodes and the porous semiconductor. The printable alumina dispersion is prepared, following the route of Weidmann et al. [101]. The morphology of the resulting porous Al_2O_3 is shown in Figure 5.15(b).

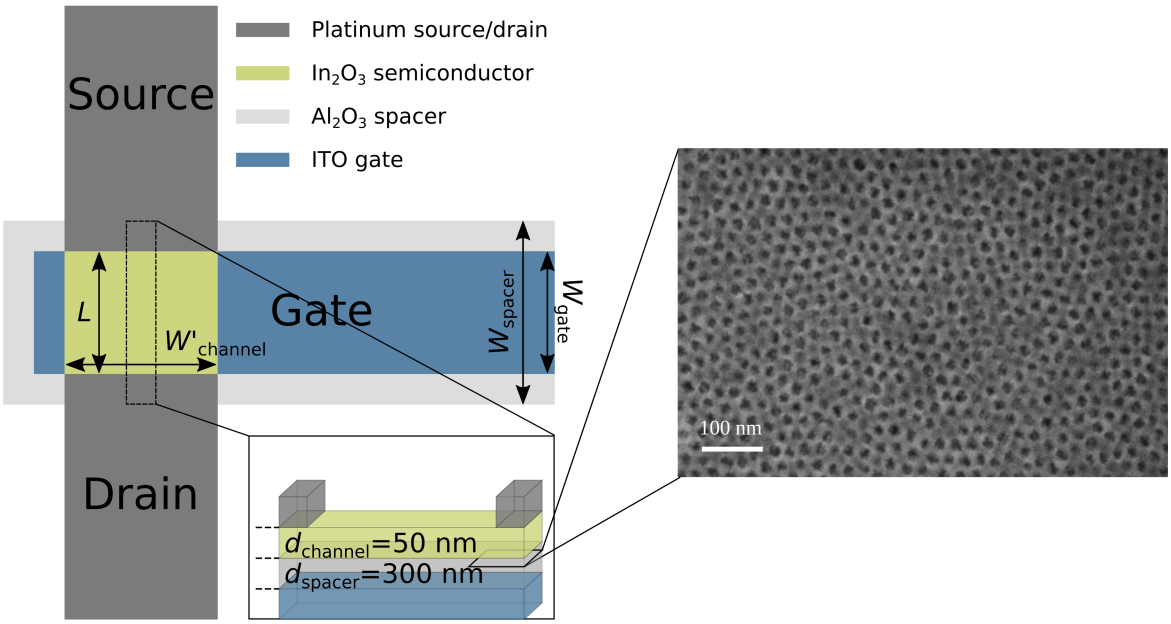


Figure 5.15.: (a) Electrolyte-gated field-effect transistor with back gate geometry. The gate electrode ($W_{gate} = 50\,\mu m$) is covered with porous Al_2O_3 ($W_{spacer} = 70\,\mu m$, $d_{spacer} = 300\,nm$) and the porous porous SnO_2 semiconductor ($W'_{channel} = L = 50\,\mu m$ and $d_{channel} = 50\,nm$) is located on top of the porous Al_2O_3 layer (see inset).(b) SEM micrograph of the porous structure of printed and calcinated Al_2O_3 network. The pore size of the Al_2O_3 network is ~20 nm.

With the device geometry as shown in Figure 5.15(a) the gate-to-channel distance can be reduced to the thickness of the porous Al_2O_3 spacer of 300 nm. This results in a much smaller resistance of the CSPE-1(sd) and thereby in a much shorter time constant τ_{RC}. In order to stack two porous films on top of each other, i.e., porous SnO_2 on top of porous Al_2O_3, one has to avoid an

infiltration of the SnO_2 precursor ink into the porous Al_2O_3 spacer. Therefore an intermediate heating step to 300 °C is performed, which is sufficient to solidify the porous Al_2O_3 structure. The polymer micelles are left intact and still fill the pores of Al_2O_3. Subsequently, the SnO_2 precursor is applied. Due to the filled pores of the Al_2O_3 the SnO_2 precursor is not able to penetrate into the Al_2O_3 pores. The final calcination is done in a single heating step utilizing the same parameters as described in section 3.3.7. After calcination the CSPE-1(lq) is printed into both layers ensuring a good electrical contact between gate electrode and the semiconductor filaments of the back-gated EG-FET. Figure 5.16 shows the transfer and output characteristics of such a back gate EG-FET. The green curve of Figure 5.16(a) thereby displays the transfer characteristics of the FET for gate voltages ranging from -0.3 V to 1.2 V. The drain current I_d ranges from below 10^{-11} A to almost 10^{-6} A. The resulting on/off-current ratio is $\sim 10^5$. The subthreshold swing of 89 mV/dec is very close to the theoretical limit of ($\sim$59 mV/dec) and indicates, that only a small number of interface trap states are present. The threshold voltage is $V_{th} = 0.39$ V and is determined as described in section 3.1.8. The device is thus a normally off device. The field-effect mobility μ_{FET} is determined from eq. 3.8, where $W = W_{channel}$ from eq. (5.4) for the changed channel geometry and C_{dl} is calculated as in eq. (5.6).

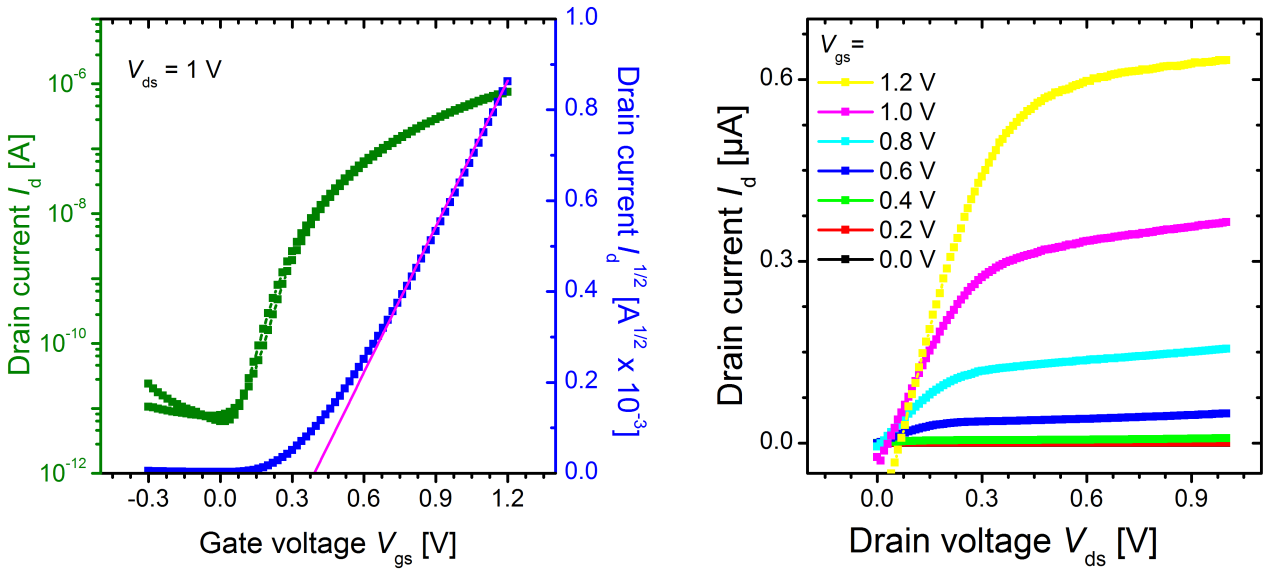


Figure 5.16.: Transfer (a) and output (b) characteristics of a back-gated EG-FET with horizontal porous SnO_2-channel.

With 4114 pillars (see appendix H), the channel width amounts to 258.5 μm. The field-effect mobility then results in 0.23 $cm^2\,V^{-1}\,s^{-1}$. This value is reduced by a factor of ten compared to the v-FET (2.2 $cm^2\,V^{-1}\,s^{-1}$). As mentioned earlier, the field-effect mobility is not a material property but a device property. The discrepancy between the mobility of the v-FETs and the back-gated

EG-FET can in this case be explained with the increased channel length. The longer the channel is, the more grain boundaries the electrons have to pass and the lower is the field-effect mobility.

Anyhow, the key advantage of the back gate geometry is the reduced gate-to-channel distance. The distance in this case is reduced to the thickness of the porous Al_2O_3 layer, which is about 300 nm but has not been optimized so far. The reduced channel to gate distance results in a >100-fold shorter time constant τ_{RC} and has the further advantage of the gate being parallel to the transistor channel. The parallel arrangement ensures a constant distance between gate and channel, instead of the strongly varying gate-to-channel distance of the v-FET. A parallel structure is thereby beneficial for the channel formation, because the resistance of the bulk of the electrolyte is constant for all locations and therewith the charging time τ_{RC} of the channel. In the in-plane gate geometry, the distance between gate and semiconductor varies for different semiconductor positions, which can cause temporally inhomogeneous charging of the channel. Another advantage realized in the back gate EG-FET geometry is the lithographically structured channel area. Unlike the v-FET, where the entire droplet is gated with CSPE-1(sd), the channel in this case is lithographically structured. If this could be applied to the v-FET, the channel capacitance could be reduced by a factor of >10000, which complies with the droplet to electrode area ratio. This would reduce the total capacitance and consequently τ_{RC} by the same factor. A lithographically structured channel was technically not realizable for the v-FET, because during lift-off of the porous SnO_2 semiconductor, the micelles were removed and the deposition of platinum for the drain electrode caused a short circuit. Still, theoretically, a back-gated v-FET with a lithographically structured channel has the potential for time constants τ_{RC} as low as 0.22 μs, which results in a maximum switching frequency of >1 MHz.

5.5 Summary

In this chapter a new vertical field-effect transistor, with a porous electrolyte driven semiconductor was introduced and realized. An optimized preparation routine for the printed semiconductor porous SnO_2 layer was developed. The semiconducting channel was comprehensively characterized using optical as well as refractive methods. The pore and crystal size was estimated and the necessary percolation of the porous network was confirmed. The v-FETs showed close to ideal transfer and output curves with extraordinary current densities of >0.1 MA/cm^{-2}. Deviations of the current densities from the simple scaling with the electrode areas were identified as a result of strong influence of stray currents and a finite penetration depth of the liquid electrolyte in the channel region. An electrolyte penetration depth of ∼300 nm into the channel area was shown to be consistent for three out of four devices with different electrode sizes and consistent with a full penetration of a 0.25 μm-device. The v-FET exhibited, on top of the very large current density, the classical ${V_{gs}}^2$ behavior of the drain current. Computer simulations performed by project partners indicated potential enhancement of the device performance by shrinking pore size and filament

width. A way for a decrease of the gate-to-channel distance by utilization of back-gate geometry was proposed and its potential suitability for a faster switching device was shown.

6 Conclusions

In the present thesis, solid polymer electrolytes as gating dielectrics for FETs have been advanced by mixing with liquid additives (solvents) exhibiting low melting temperatures. The resulting composite solid polymer electrolytes (CSPEs) partially retain the liquid phase of the additives even in the solidified state. The advantages of such CSPEs are easy inkjet printability, high gating efficiency and the possibility to fabricate miniaturized, fast and temperature insensitive FETs. In this context three different field-effect transistor geometries comprising a horizontal channel FET, a vertical channel FET both with in-plane gate geometry and a horizontal channel FET with back gate geometry all utilizing an optimized CSPE have been developed and electrically characterized.

To examine the temperature stability of the CSPE with respect to an application in an electrolyte-gated FET (EG-FET) three different CSPE compositions have been tested chemically, mechanically and electrically. In a drying study the presence of a liquid phase in the solidified electrolyte was confirmed. On the one hand this is beneficial for the ionic conductivity of the CSPEs but on the other hand it also raises questions about its physical state at low temperatures and its mechanical stability. Differential scanning calorimetry measurements indicated, that no phase transition takes place for the simplest CSPE (CSPE-1 composed of $LiClO_4$, PVA[1], PC[2] and DMSO[3]) containing the solvent with the highest melting temperature. The other CSPEs were considered to behave likewise. The electrical characterization of all three CSPEs was done using impedance spectroscopy employing a CSPE filled parallel plate capacitor. To this end, a representative equivalent circuit has been developed, which allowed to extract the ionic conductivity σ_{el} as well as the areal double layer capacitance C_{dl}, two key parameters for the electrical performance of the CSPEs in electrolyte-gated FETs. Measurements have been conducted at discrete temperatures between -45 °C and +45 °C. They showed an expected increase of σ_{el} of about two orders of magnitude and at the same time an unexpected increase of C_{dl} with temperature of about 50 %. This increase was surprising since an increase of the solvation shell radius of the ions, as stated in the Stokes-Einstein equation would result in a reduced capacitance with increasing temperature. To elucidate this phenomenon, the possibility of crystallization of the included $LiClO_4$ salt during the solidification process has been considered followed by a dissociation of the salt at increased temperatures due to higher solubility. XRD studies on the CSPE(sd) indicated no characteristic reflections for $LiClO_4$ and impedance measurements on highly diluted as well as

[1] polyvinyl alcohol
[2] propylene carbonate
[3] dimethyl sulfoxide

supersaturated solutions showed both the same temperature behavior as the CSPEs(sd), which proved this hypothesis wrong. Another reason for the increasing C_{dl} could be a reduced binding energy of the solvation shell due to the increased temperature, which results in a closer approach of the ions to the electrode. Also a combination of the reduced binding energy with temperature and the presence of counter charges in the electrodes would diminish the need for the solvation shell for ions approaching the interface. This would explain the positive trend of the areal capacitance with temperature. After a thorough analysis of the chemical and electrical properties with temperature, CSPE-1 is found to be the superior solid electrolyte in terms of ionic conductivity and areal double layer capacitance over the entire investigated temperature range.

Utilizing CSPE-1, an FET was fabricated and characterized at different working temperatures. From the Shockley equations the dependence of $I_{\mathrm{d,on}}$ on the threshold voltage V_{th}, the electric double layer C_{dl} and the mobility μ_{FET} is derived. Two parameters are particularly noticeable, namely V_{th} and the on-current $I_{\mathrm{d,on}}$. Both parameters were found to be almost temperature independent. For the threshold voltage this behavior is not too surprising, because from theory only a very small shift $<0.7\,\mathrm{mV\,K^{-1}}$ is expected. The constant on-current with temperature on the other hand turned out to be a beneficial interplay of two factors. For a constant V_{th}, the increase of C_{dl} is compensated by a likewise decrease of μ_{FET}. The rising number of phonons in the semiconductor crystal with temperature caused μ_{FET} to decrease in a way, compensating for the increase of C_{dl}. Anyhow, the temperature insensitive V_{th} and $I_{\mathrm{d,on}}$ are very beneficial for future applications of CSPEs in logics electrical circuits and everyday applications.

In order to realize the miniaturization of EG-FETs combined with large on-currents, an entirely new concept of a vertical channel field-effect transistor (v-FET) was developed. The idea of utilizing a porous semiconductor as large area channel material gated by a CSPE makes it necessary to carefully optimize the mixture of the SnO_2 precursor ink with using a polymer with the ability to form micelles and its calcination routine. To get the right pore size and filament width of the semiconductor network was as important as the realization of the interconnecting pore network to guarantee the infiltration of the CSPE(lq). Different polymers with the ability to form micelles were tested as ingredient of the SnO_2 precursors and calcined at different temperatures for different times. The optimal structure was synthesized from a (P/E/B)-*b*-(PEO) containing SnO_2 precursor ink after calcination at 550 °C for 5 minutes. The final product was a polycrystalline porous structure composed of nanocrystals with diameters ranging from 3 to 5 nm and pore sizes as well as filament widths of ∼20 nm. From an electron tomography a three dimensional picture of the semiconductor network proved good interconnectivity of the pores in the SnO_2 network. Additionally, the semiconductor to pore ratio was determined to 52 : 48. A printed film of this precursor in between two platinum electrodes was used for the vertically stacked (source-channel-drain) FET. With this layer sequence and in-plane gate geometry an electrolyte-gated vertical channel FET with a printed channel was realized for the first time. The electrical analysis necessitated some judicious approximations. Since the channel surface could not be determined experimentally, the

porous SnO_2 network was modeled by an array of pillars with the semiconductor to pore ratio determined by electron tomography. The pillar diameter of 20 nm was taken from the filament width and the channel length of 45 nm from the film thickness. These values were used to calculate the channel width. All characteristic FET parameters were determined, among others, the field-effect mobility and the on-current density. The electrical characterization of devices with increasing channel widths (synonymous for a larger electrode area) yields a reduced on-current density, which, according to the Shockley equations, should be constant for ideal devices. In an attempt to explain this discrepancy two hypothesizes were tested. The first hypothesis was the influence of stray currents flowing through the semiconductor regions outside of the electrode area. The second one considers a finite penetration depth of the CSPE under the electrode area due to the repelling forces of enclosed and trapped air in the center part of the electrode area. Concerning the stray currents it was found that especially for small electrode sizes (<300 nm) a considerable amount of current, namely >30 % of the total current, flows through the outside of the electrode area. With increasing electrode areas this ratio decays fast. This correction was not able to describe this phenomenon satisfactorily. Considering the results of the first hypothesis, the second hypothesis of limited CSPE penetration depth in the active porous semiconductor volume was able to explain the reduction of the current density for three out of four device geometries, namely 0.25 μm-, 1 μm- and 2 μm-devices. The assumption of a fixed penetration depth of $\sim$0.3 μm turned out to be consistent with a fully penetrated 0.25 μm-device. The latter device thereby shows almost ideal transistor characteristics and its derived electrical key parameters were used in drift diffusion simulations conducted with project partners. The simulated characteristics showed a good match with the experimental characteristics validating the derived experimental parameters and additionally showing potential for further optimization.

One of the key features of the horizontal and the vertical channel FET geometries is their in-plane gate geometry, which made the printing of CSPE(lq) onto channel and gate electrode comparatively easy. However, as a side effect, it also enlarges the total device area and reduces the switching speed due to the large channel to gate distance of $\sim$50 μm. A novel approach utilizing back-gate geometry reduces this distance and additionally ensures a constant channel to gate distance, which is not the case for in-plane geometry. A porous Al_2O_3 network with a thickness of about 300 nm was used as a spacer to create a spatial separation of the bottom gate and the porous channel. Compared to the in-plane geometry it improves the switching speed by more than two orders of magnitude.

7 Future Experiments

A logical continuation of the mainly theoretically covered switching speed of the FETs would be conducting further experiments on this topic. Only few devices were measured to check for the time constants of the FETs and the correctness of the calculated values. A comprehensive study to check for the time constants of the v-FET and the back gated FET would be very interesting also for their application in logics and circuits.

The v-FETs, even though they showed close to ideal transistor behavior for small electrode areas, suffered from limited penetration depths for larger electrode areas. To exploit the full potential in terms of current density this problem has to be overcome. A solution for such problem could be provided by porous electrode materials allowing an easier access for the CSPE, the trapped air to escape and to fill the channel volume completely.

During the impedance spectroscopy experiments an increase of double layer capacitance was recognized, which was not understood entirely. Additionally, an unknown component showed up, which was described with a Warburg element. This contribution, even tough it is not influencing the conductivity or double layer capacitance, is not understood in detail and would be very interesting to investigate. Also the positive temperature behavior of the double layer capacitance is worth investigating in more detail. Pursuing experiments to understand these effect could give further insight into the basic functionality of the CSPEs and are probably of interest for the whole electrolyte community.

Bibliography

[1] American Printing History Association. To Encourage the Study of Printing History, 2015.

[2] Suresh Kumar Garlapati, Tessy Theres Baby, Simone Dehm, Mohammed Hammad, Venkata Sai Kiran Chakravadhanula, Robert Kruk, Horst Hahn, and Subho Dasgupta. Ink-Jet Printed CMOS Electronics from Oxide Semiconductors. *Small (Weinheim an der Bergstrasse, Germany)*, 11(29):3591–6, aug 2015.

[3] Ping-Hei Chen, Wen-Cheng Chen, and S.-H. Chang. Bubble growth and ink ejection process of a thermal ink jet printhead. *International Journal of Mechanical Sciences*, 39(6):683–695, 1997.

[4] Ping-Hei Chen, Hsin-Yah Peng, Hsin-Yi Liu, S.-L. Chang, T.-I. Wu, and Chiang-Ho Cheng. Pressure response and droplet ejection of a piezoelectric inkjet printhead. *International Journal of Mechanical Sciences*, 41(2):235–248, 1999.

[5] D J Hayes, M E Grove, D B Wallace, T Chen, and W R Cox. Ink-jet printing in the manufacturing of electronics, photonics, and displays. In Guozhong Cao and Wiley P. Kirk, editors, *Proceedings of SPIE - The International Society for Optical Engineering*, volume 4809, pages 94–99. International Society for Optics and Photonics, nov 2002.

[6] H Sirringhaus, T Kawase, R H Friend, T Shimoda, M Inbasekaran, W Wu, and E P Woo. High-Resolution Inkjet Printing of All-Polymer Transistor Circuits. *Science*, 290(5499):2123–2126, dec 2000.

[7] T Kawase, H Sirringhaus, R H Friend, and T Shimoda. All-Polymer Thin Film Transistors Fabricated by Inkjet Printing. *Proceedings of the SPIE - Organic Field Effect Transistors*, 4466(1):80–88, 2001.

[8] Ba Ridley, B Nivi, and Jm Jacobson. All-Inorganic Field Effect Transistors Fabricated by Printing. *Science (New York, N.Y.)*, 286(5440):746–749, oct 1999.

[9] Sawyer B Fuller, Eric J Wilhelm, and Joseph M Jacobson. Ink-Jet Printed Nanoparticle Microelectromechanical Systems. *Journal of Microelectromechanical Systems*, 11(1):54–60, 2002.

[10] T. Kawase, H. Sirringhaus, R. H. Friend, and T. Shimoda. Inkjet printed via-hole interconnections and resistors for all-polymer transistor circuits. *Advanced Materials*, 13(21):1601–1605, nov 2001.

[11] Ali Afzali, Christos D. Dimitrakopoulos, and Tricia L. Breen. High-performance, solution-processed organic thin film transistors from a novel pentacene precursor. *Journal of the American Chemical Society*, 124(30):8812–8813, 2002.

[12] Gregor G. Rozenberg, Eric Bresler, Stuart P. Speakman, Chris Jeynes, and Joachim H G Steinke. Patterned low temperature copper-rich deposits using inkjet printing. *Applied Physics Letters*, 81(27):5249–5251, 2002.

[13] Kateri E. Paul, William S. Wong, Steven E. Ready, and Robert A. Street. Additive jet printing of polymer thin-film transistors. *Applied Physics Letters*, 83(10):2070–2072, 2003.

[14] Giuseppina Polino, Robert Abbel, Santhosh Shanmugam, Guy J P Bex, Rob Hendriks, Francesca Brunetti, Aldo Di Carlo, Ronn Andriessen, and Yulia Galagan. A benchmark study of commercially available copper nanoparticle inks for application in organic electronic devices. *Organic Electronics: physics, materials, applications*, 34:130–138, 2016.

[15] Michela Borghetti, Mauro Serpelloni, Emilio Sardini, and Stefano Pandini. Mechanical behavior of strain sensors based on PEDOT:PSS and silver nanoparticles inks deposited on polymer substrate by inkjet printing. *Sensors and Actuators, A: Physical*, 243:71–80, 2016.

[16] Po-Chin Yu, Chien-Chong Hong, and Tong-Miin Liou. Bendable transparent conductive meshes based on multi-layer inkjet-printed silver patterns. *Journal of Micromechanics and Microengineering*, 26(3):035012, mar 2016.

[17] Andreas Albrecht, Almudena Rivadeneyra, Alaa Abdellah, Paolo Lugli, and F Salmero. Inkjet printing and photonic sintering of silver and copper oxide nanoparticles for ultra-low-cost condctive patterns. *Journal of Materials Chemistry C*, 4(16):3546–3554, 2016.

[18] G. Vescio, J. López-Vidrier, R. Leghrib, A. Cornet, and A. Cirera. Flexible inkjet printed high-k HfO 2 -based MIM capacitors. *J. Mater. Chem. C*, 4(9):1804–1812, 2016.

[19] Tessy T. Baby, Suresh K. Garlapati, Simone Dehm, Marc Häming, Robert Kruk, Horst Hahn, and Subho Dasgupta. A general route toward complete room temperature processing of printed and high performance oxide electronics. *ACS Nano*, 9(3):3075–3083, 2015.

[20] Suresh Kumar Garlapati, Nilesha Mishra, Simone Dehm, Ramona Hahn, Robert Kruk, Horst Hahn, and Subho Dasgupta. Electrolyte-gated, high mobility inorganic oxide transistors from printed metal halides. *ACS Applied Materials and Interfaces*, 5(22):11498–11502, 2013.

[21] S Dasgupta, S Gottschalk, R Kruk, and H Hahn. A nanoparticulate indium tin oxide field-effect transistor with solid electrolyte gating. *Nanotechnology*, 19(43):435203, oct 2008.

[22] Subho Dasgupta, Robert Kruk, Norman Mechau, and Horst Hahn. Inkjet printed, high mobility inorganic-oxide field effect transistors processed at room temperature. *ACS Nano*, 5(12):9628–9638, 2011.

[23] Subho Dasgupta, Ganna Stoesser, Nina Schweikert, Ramona Hahn, Simone Dehm, Robert Kruk, and Horst Hahn. Printed and electrochemically gated, high-mobility, inorganic oxide nanoparticle FETs and their suitability for high-frequency applications. *Advanced Functional Materials*, 22(23):4909–4919, dec 2012.

[24] Masanobu Tanaka, Youji Mabuchi, Tomohiro Hayashi, and Masahiko Hara. Subtractive offset printing for fabrication of sub micrometer scale electrodes with gold nanoparticles. *Microelectronic Engineering*, 95:14–20, 2012.

[25] Young Hun Han, Ju Yeon Won, Hyun Seok Yoo, Jae Hyun Kim, Rino Choi, and Jae Kyeong Jeong. High Performance Metal Oxide Field-Effect Transistors with a Reverse Offset Printed Cu Source/Drain Electrode. *ACS Applied Materials and Interfaces*, 8(2):1156–1163, 2016.

[26] Jaakko Leppäniemi, Olli Heikki Huttunen, Himadri Majumdar, and Ari Alastalo. Flexography-Printed In2O3 Semiconductor Layers for High-Mobility Thin-Film Transistors on Flexible Plastic Substrate. *Advanced Materials*, 27(44):7168–7175, nov 2015.

[27] Michihiko Maeda, Jun Hirotani, Ryotaro Matsui, Kentaro Higuchi, Shigeru Kishimoto, Takuya Tomura, Masafumi Takesue, Katsuhiko Hata, and Yutaka Ohno. Printed, short-channel, top-gate carbon nanotube thin-film transistors on flexible plastic film. *Applied Physics Express*, 8(4), 2015.

[28] Radoslav Parashkov, Eike Becker, Thomas Riedl, Hans Hermann Johannes, and Wolfgang Kowalsky. Large area electronics using printing methods. *Proceedings of the IEEE*, 93(7):1321–1329, jul 2005.

[29] Do Hyung Kim, Sung Soo Ryu, Dongwook Shin, Jung Han Shin, Jwa Jin Jeong, Hyeong Jun Kim, and Hyo Sik Chang. The fabrication of front electrodes of Si solar cell by dispensing printing. *Materials Science and Engineering B: Solid-State Materials for Advanced Technology*, 177(2):217–222, 2012.

[30] Denis Erath, Aleksander Filipović, Marc Retzlaff, Anne Kathrin Goetz, Florian Clement, Daniel Biro, and Ralf Preu. Advanced screen printing technique for high definition front side metallization of crystalline silicon solar cells. *Solar Energy Materials and Solar Cells*, 94(1):57–61, 2010.

[31] David Mühlbacher, Markus Scharber, Mauro Morana, Zhengguo Zhu, David Waller, Russel Gaudiana, and Christoph Brabec. High photovoltaic performance of a low-bandgap polymer. *Advanced Materials*, 18(21):2884–2889, 2006.

[32] Nicolas Blouin, Alexandre Michaud, and Mario Leclerc. A low-bandgap poly(2,7-carbazole) derivative for use in high-performance solar cells. *Advanced Materials*, 19(17):2295–2300, 2007.

[33] J Peet, J Y Kim, N E Coates, W L Ma, D Moses, A J Heeger, and G C Bazan. Efficiency enhancement in low-bandgap polymer solar cells by processing with alkane dithiols. *Nature Materials*, 6(7):497–500, 2007.

[34] S H Park, A Roy, S Beaupré, S Cho, N Coates, J S Moon, D Moses, M Leclerc, K Lee, S Beaupre, and A J Heeger. Bulk heterojunction solar cells with internal quantum efficiency approaching 100%. *Nature Photon.*, 3(5):297–302, 2009.

[35] Naveed Khan, Ayesha Kausar, and Amin Ur Rahman. Modern Drifts in Conjugated Polymers and Nanocomposites for Organic Solar Cells : A Review Modern Drifts in Conjugated Polymers and Nanocomposites for Organic Solar Cells : A Review. *Polymer-Plastics Technology and Engineering*, 2559(June 2016):140–154, 2015.

[36] Frederik C. Krebs. Fabrication and processing of polymer solar cells: A review of printing and coating techniques. *Solar Energy Materials and Solar Cells*, 93(4):394–412, 2009.

[37] Han-Ki Kim, In-Kyu You, Jae Bon Koo, and Sung-Ho Kim. Organic solar cells fabricated on inkjet-printed indium tin oxide electrodes. *Surface and Coatings Technology*, 211:33–36, 2012.

[38] Jin-A. Jeong, Jinho Lee, Hongdoo Kim, Han-Ki Kim, and Seok-In Na. Ink-jet printed transparent electrode using nano-size indium tin oxide particles for organic photovoltaics. 2010.

[39] Chunhe Yang, Erjun Zhou, Shoji Miyanishi, Kazuhito Hashimoto, and Keisuke Tajima. Preparation of active layers in polymer solar cells by aerosol jet printing. *ACS Applied Materials and Interfaces*, 3(10):4053–4058, 2011.

[40] Ruth Cherrington, Darren J. Hughes, S. Senthilarasu, and Vannessa Goodship. Inkjet-Printed TiO ₂ Nanoparticles from Aqueous Solutions for Dye-Sensitized Solar Cells (DSSCs). *Energy Technology*, 3(8):866–870, 2015.

[41] Syed Ghufran Hashmi, Merve Ozkan, Janne Halme, Katarina Dimic Misic, Shaik Mohammed Zakeeruddin, Jouni Paltakari, Michael Grätzel, and Peter D. Lund. High performance dye-sensitized solar cells with inkjet printed ionic liquid electrolyte. *Nano Energy*, 17:206–215, 2015.

[42] Syed Ghufran Hashmi, Merve Özkan, Janne Halme, Shaik Mohammed Zakeeruddin, Jouni Paltakari, Michael Grätzel, and Peter D. Lund. Dye-sensitized solar cells with inkjet-printed dyes. *Energy Environ. Sci.*, 9:2453–2462, 2016.

[43] David Dodoo-Arhin, Richard C.T. Howe, Guohua Hu, Yinghe Zhang, Pritesh Hiralal, Abdulhakeem Bello, Gehan Amaratunga, and Tawfique Hasan. Inkjet-printed graphene electrodes for dye-sensitized solar cells. *Carbon*, 105:33–41, 2016.

[44] Sean Xia, Kwang-Ohk Cheon, Jason J. Brooks, Mark Rothman, Tan Ngo, Patrick Hett, Raymond C. Kwong, Mike Inbasekaran, Julie J. Brown, Takuya Sonoyama, Masaki Ito, Shunichi Seki, and Satoru Miyashita. Printable phosphorescent organic light-emitting devices. *Journal of the Society for Information Display*, 2008(2):167–172, 2009.

[45] D. H. Lee, J. S. Choi, H. Chae, C. H. Chung, and S. M. Cho. Screen-printed white OLED based on polystyrene as a host polymer. *Current Applied Physics*, 9(1):161–164, jan 2009.

[46] Hongzheng Jin and James C. Sturm. Super-high-resolution transfer printing for full-color OLED display patterning. *Journal of the Society for Information Display*, 18(2):141, 2010.

[47] Aran Kim, Hyemi Lee, Choonghan Ryu, Sung Min Cho, and Heeyeop Chae. Nanoscale Thickness and Roughness Control of Gravure Printed MEH-PPV Layer by Solvent Printing for Organic Light Emitting Diode. *Journal of Nanoscience and Nanotechnology*, 10(5):3326–3330, 2010.

[48] Fei Fei, Jinyong Zhuang, Weichen Wu, Minshun Song, Dongyu Zhang, Sen Li, Wenming Su, and Zheng Cui. A printed aluminum cathode with low sintering temperature for organic light-emitting diodes. *RSC Adv.*, 5(1):608–611, 2015.

[49] Anand Verma, Daniel M. Zink, Charlotte Fléchon, Jaime Leganés Carballo, Harald Flügge, José M. Navarro, Thomas Baumann, and Daniel Volz. Efficient, inkjet-printed TADF-OLEDs with an ultra-soluble NHetPHOS complex. *Applied Physics A: Materials Science and Processing*, 122(3):1–5, 2016.

[50] Mingjing Ha, Yu Xia, Alexander A. Green, Wei Zhang, Mike J. Renn, Chris H. Kim, Mark C. Hersam, and C. Daniel Frisbie. Printed, sub-3V digital circuits on plastic from aqueous carbon nanotube inks. *ACS Nano*, 4(8):4388–4395, 2010.

[51] Mingjing Ha, Jung Woo T Seo, Pradyumna L. Prabhumirashi, Wei Zhang, Michael L. Geier, Michael J. Renn, Chris H. Kim, Mark C. Hersam, and C. Daniel Frisbie. Aerosol jet printed, low voltage, electrolyte gated carbon nanotube ring oscillators with sub-5 µs stage delays. *Nano Letters*, 13(3):954–960, 2013.

[52] Felice Torrisi, Tawfique Hasan, Weiping Wu, Zhipei Sun, Antonio Lombardo, Tero S. Kulmala, Gen Wen Hsieh, Sungjune Jung, Francesco Bonaccorso, Philip J. Paul, Daping Chu, and Andrea C. Ferrari. Inkjet-printed graphene electronics. *ACS Nano*, 6(4):2992–3006, apr 2012.

[53] Tran Quang Trung, Nguyen Thanh Tien, Doil Kim, Mi Jang, Ok Ja Yoon, and Nae-Eung Lee. A Flexible Reduced Graphene Oxide Field-Effect Transistor for Ultrasensitive Strain Sensing. *Advanced Functional Materials*, 24(1):117–124, jan 2014.

[54] Abhilash Thanniyil Sebastian, Roberto De Alba, Nikolay Zhelev, Harold Craighead, and Jeevak Parpia. Transfer Printing of CVD Graphene FETs on Patterned Substrates. *Nanoscale*, pages 14109–14113, 2015.

[55] Freddy G. Del Pozo, Simone Fabiano, Raphael Pfattner, Stamatis Georgakopoulos, Sergi Galindo, Xianjie Liu, Slawomir Braun, Mats Fahlman, Jaume Veciana, Concepció Rovira, Xavier Crispin, Magnus Berggren, and Marta Mas-Torrent. Single crystal-like performance in solution-coated thin-film organic field-effect transistors. *Advanced Functional Materials*, 26(14):2379–2386, apr 2016.

[56] Yongbo Yuan, Gaurav Giri, Alexander L Ayzner, Arjan P Zoombelt, Stefan C B Mannsfeld, Jihua Chen, Dennis Nordlund, Michael F Toney, Jinsong Huang, and Zhenan Bao. Ultra-high mobility transparent organic thin film transistors grown by an off-centre spin-coating method. *Nature communications*, 5:3005, jan 2014.

[57] Hsin Rong Tseng, Hung Phan, Chan Luo, Ming Wang, Louis A. Perez, Shrayesh N. Patel, Lei Ying, Edward J. Kramer, Thuc Quyen Nguyen, Guillermo C. Bazan, and Alan J. Heeger. High-mobility field-effect transistors fabricated with macroscopic aligned semiconducting polymers. *Advanced Materials*, 26(19):2993–2998, 2014.

[58] Paul S.K. Amegadze and Yong-Young Noh. Development of high-performance n-type organic thin-film transistors using a small-molecule polymer blend. *Thin Solid Films*, 556:414–418, 2014.

[59] Babak Nasr, Zhirong Zhao-Karger, Di Wang, Robert Kruk, Horst Hahn, and Subho Dasgupta. Temperature tolerance study of high performance electrochemically gated SnO2 nanowire field-effect transistors. *Journal of Materials Chemistry C*, 1(14):2534, 2013.

[60] Suresh Kumar Garlapati. to be published. 2017.

[61] S. M. Sze and K. K. Ng. Physics of Semiconductor Devices, 3rd Edition - Simon M. Sze, Kwok K. Ng. *Physics of Semiconductor Devices, 3rd Edition.; John Wiley & Sons, Inc.; NJ*, pages 164, 682, 2007.

[62] Roland Schmechel, Aline Hepp, Holger Heil, Marcus Ahles, Wieland Weise, and Heinz von Seggern. Light-emitting field-effect transistor: simple model and underlying functional mechanisms. page 101, nov 2003.

[63] Yasutaka Uchida, Yoshiaki Watanabe, Masaru Takabatake, and Masakiyo Matsumura. Vertical-Type Amorphous-Silicon Field-Effect Transistors with Small Parasitic Elements. *Japanese Journal of Applied Physics*, 25(9):798–800, 1986.

[64] Hou T. Ng, J. Han, Toshishige Yamada, P. Nguyen, Yi P. Chen, and M. Meyyappan. Single Crystal Nanowire Vertical Surround-Gate Field-Effect Transistor. *Nano Letters*, 4(7):1247–1252, jul 2004.

[65] M Egard, S Johansson, A.-C. Johansson, K-M Persson, a W Dey, B M Borg, C Thelander, L-E Wernersson, and E Lind. Vertical InAs Nanowire Wrap Gate Transistors with f t > 7 GHz and f max > 20 GHz. *Nano Letters*, 10(3):809–812, mar 2010.

[66] K Tomioka, M Yoshimura, and T Fukui. A III-V nanowire channel on silicon for high-performance vertical transistors. *Nature*, 488(7410):189–192, 2012.

[67] Woo Jong Yu, Zheng Li, Hailong Zhou, Yu Chen, Yang Wang, Yu Huang, and Xiangfeng Duan. Vertically stacked multi-heterostructures of layered materials for logic transistors and complementary inverters. *Nature materials*, 12(3):246–52, 2013.

[68] Se Hyun Kim, Kihyon Hong, Wei Xie, Keun Hyung Lee, Sipei Zhang, Timothy P. Lodge, and C. Daniel Frisbie. Electrolyte-gated transistors for organic and printed electronics, apr 2013.

[69] Matthew J. Panzer and C. Daniel Frisbie. Polymer electrolyte-gated organic field-effect transistors: Low-voltage, high-current switches for organic electronics and testbeds for probing electrical transport at high charge carrier density. *Journal of the American Chemical Society*, 129(20):6599–6607, 2007.

[70] Lars Herlogsson, Xavier Crispin, Nathaniel D. Robinson, Mats Sandberg, Olle Jonny Hagel, Göran Gustafsson, and Magnus Berggren. Low-voltage polymer field-effect transistors gated via a proton conductor. *Advanced Materials*, 19(1):97–101, 2007.

[71] Robert J Klein, Shihai Zhang, Shichen Dou, Brad H Jones, Ralph H Colby, and James Runt. Modeling electrode polarization in dielectric spectroscopy: Ion mobility and mobile ion concentration of single-ion polymer electrolytes. *The Journal of Chemical Physics*, 124(14):144903, apr 2006.

[72] Saumya R. Mohapatra, T. Tsuruoka, T. Hasegawa, K. Terabe, and M. Aono. Flexible resistive switching memory using inkjet printing of a solid polymer electrolyte. *AIP Advances*, 2(2):022144, 2012.

[73] Kihyon Hong, Se Hyun Kim, Ankit Mahajan, and C. Daniel Frisbie. Aerosol jet printed p- and n-type electrolyte-gated transistors with a variety of electrode materials: Exploring practical routes to printed electronics. *ACS Applied Materials and Interfaces*, 6(21):18704–18711, 2014.

[74] Torsten Brezesinski, Anna Fischer, Ken Ichi Iimura, Clément Sanchez, David Grosso, Markus Antonietti, and Bernd M. Smarsly. Generation of self-assembled 3D mesostructured SnO2

thin films with highly crystalline frameworks. *Advanced Functional Materials*, 16(11):1433–1440, jul 2006.

[75] Falk Von Seggern, Inna Keskin, Erin Koos, Robert Kruk, Horst Hahn, and Subho Dasgupta. Temperature-dependent performance of printed field-effect transistors with solid polymer electrolyte gating. *ACS Applied Materials and Interfaces*, 8(46):31757–31763, nov 2016.

[76] M. Marzantowicz, J. R. Dygas, F. Krok, A. Łasińska, Z. Florjańczyk, and E. Zygadło-Monikowska. In situ microscope and impedance study of polymer electrolytes. *Electrochimica Acta*, 51(8-9):1713–1727, 2006.

[77] Hans Vogel. The law of the relation between the viscosity of liquids and the temperature. *Physikalische Zeitschrift*, 22:645–646, 1921.

[78] G. Tammann. Glasses as supercooled liquids. *Journal of the Society of Glass Technology*, 9:166–185, 1925.

[79] G. S. Fulcher. Analysis of recent measurements of the viscosity of glasses. *Journal of the American Ceramic Society*, 8:339–355, 1925.

[80] P.E Stallworth, J.J Fontanella, M.C Wintersgill, Christopher D Scheidler, Jeffrey J Immel, S.G Greenbaum, and A.S Gozdz. NMR, DSC and high pressure electrical conductivity studies of liquid and hybrid electrolytes. *Journal of Power Sources*, 81-82:739–747, 1999.

[81] Yongwoo Kwon and Byoungnam Park. Subthreshold slope as a measure of interfacial trap density in pentacene films. *Thin Solid Films*, 599:145–150, jan 2016.

[82] Yuan Taur and Tak H. Ning. *Fundamentals of Modern VLSI Devices*. Cambridge University Press, New York, 9th edition, 1998.

[83] Harald Ibach and Hans Lüth. *Festköperphysik: Einführung in die Grundlagen*. 2009.

[84] Takeshi Niitani, Mikiya Shimada, Kiyoshi Kawamura, and Kiyoshi Kanamura. Characteristics of new-type solid polymer electrolyte controlling nano-structure. *Journal of Power Sources*, 146(1-2):386–390, aug 2005.

[85] Chen Zhao, Caiyun Wang, Zhilian Yue, Kewei Shu, and Gordon G. Wallace. Intrinsically Stretchable Supercapacitors Composed of Polypyrrole Electrodes and Highly Stretchable Gel Electrolyte. *ACS Applied Materials & Interfaces*, 5(18):9008–9014, sep 2013.

[86] Taylor Kelly, Bahar Moradi Ghadi, Sean Berg, and Haleh Ardebili. In Situ Study of Strain-Dependent Ion Conductivity of Stretchable Polyethylene Oxide Electrolyte. *Scientific Reports*, 6:20128, feb 2016.

[87] Tessy Theres Baby, Manuel Rommel, Falk von Seggern, Pascal Friederich, Christian Reitz, Simone Dehm, Christian Kübel, Wolfgang Wenzel, Horst Hahn, and Subho Dasgupta. Sub-50 nm Channel Vertical Field-Effect Transistors using Conventional Ink-Jet Printing. *Advanced Materials*, 29(4):1603858, jan 2017.

[88] Stefano Roddaro, Kristian Nilsson, Gvidas Astromskas, Lars Samuelson, Lars Erik Wernersson, Olov Karlström, and Andreas Wacker. InAs nanowire metal-oxide-semiconductor capacitors. *Applied Physics Letters*, 92(25):2006–2009, 2008.

[89] Hidekazu Shimotani, Haruhiko Asanuma, Atsushi Tsukazaki, Akira Ohtomo, Masashi Kawasaki, and Yoshihiro Iwasa. Insulator-to-metal transition in ZnO by electric double layer gating. *Applied Physics Letters*, 91(8):92–95, 2007.

[90] T. Uemura, R. Hirahara, Y. Tominari, S. Ono, S. Seki, and J. Takeya. Electronic functionalization of solid-to-liquid interfaces between organic semiconductors and ionic liquids: Realization of very high performance organic single-crystal transistors. *Applied Physics Letters*, 93(26):2006–2009, 2008.

[91] S. Ono, N. Minder, Z. Chen, A. Facchetti, and A. F. Morpurgo. High-performance n -type organic field-effect transistors with ionic liquid gates. *Applied Physics Letters*, 97(14):95–98, 2010.

[92] P G Dzhavakhidze, A A Kornyshev, and Lieb. Theory of second-harmonic generation at the metal-electrolyte interface. *Physical Review*, 45(16):9339–9346, 1992.

[93] Z.M. Jarzebski and J.P. Marton. Physical Properties of SnO2 Materials II. Electrical Properties. *Journal of the Electrochemical Society*, 123(9):299C–310C, 1976.

[94] Maxime G Lemaitre, Evan P Donoghue, Mitchell a Mccarthy, Bo Liu, Sefaattin Tongay, Brent Gila, Purushottam Kumar, Rajiv K Singh, Bill R Appleton, and Andrew G Rinzler. Improved Transfer of Graphene for Organic , Field-Effect Transistors. *ACS nano*, 6(10):9095–9102, 2012.

[95] Martin Schidleja, Christian Melzer, and Heinz von Seggern. Investigation of Charge-Carrier Injection in Ambipolar Organic Light-Emitting Field-Effect Transistors. *Advanced Materials*, 21(10-11):1172–1176, mar 2009.

[96] T. Tharsika, A. Haseeb, Sheikh Akbar, Mohd Sabri, and Wong Hoong. Enhanced Ethanol Gas Sensing Properties of SnO2-Core/ZnO-Shell Nanostructures. *Sensors*, 14(8):14586–14600, aug 2014.

[97] D. E. Eastman. Photoelectric work functions of transition, rare-earth, and noble metals. *Physical Review B*, 2(1):1–2, 1970.

[98] D F Crabtree, R N S M Mehdi, and D a Wright. Electron mobility and infra-red absorption in reduced tin oxide crystals. *Methods*, 2:1503–1505, 1969.

[99] A. Oprea, E. Moretton, N. Bârsan, W. J. Becker, J. Wöllenstein, and U. Weimar. Conduction model of SnO2 thin films based on conductance and Hall effect measurements. *Journal of Applied Physics*, 100(3), 2006.

[100] Ian C. Bourg and Garrison Sposito. Molecular dynamics simulations of the electrical double layer on smectite surfaces contacting concentrated mixed electrolyte (NaCl-CaCl2) solutions. *Journal of Colloid and Interface Science*, 360(2):701–715, 2011.

[101] Christoph Weidmann, Kirstin Brezesinski, Christian Suchomski, Kristin Tropp, Natascha Grosser, Jan Haetge, Bernd M. Smarsly, and Torsten Brezesinski. Morphology-Controlled Synthesis of Nanocrystalline η-Al 2 O 3 Thin Films, Powders, Microbeads, and Nanofibers with Tunable Pore Sizes from Preformed Oligomeric Oxo-Hydroxo Building Blocks. *Chemistry of Materials*, 24(3):486–494, feb 2012.

[102] Xian-Lei Hu, Gao-Ming Hou, Ming-Qiu Zhang, Min-Zhi Rong, Wen-Hong Ruan, and Emmanuel P. Giannelis. A new nanocomposite polymer electrolyte based on poly(vinyl alcohol) incorporating hypergrafted nano-silica. *Journal of Materials Chemistry*, 22(36):18961, 2012.

Erklärung zur Dissertation

Hiermit versichere ich, die vorliegende Dissertation ohne Hilfe Dritter nur mit den angegebenen Quellen und Hilfsmitteln angefertigt zu haben. Alle Stellen, die aus Quellen entnommen wurden, sind als solche kenntlich gemacht. Diese Arbeit hat in gleicher oder ähnlicher Form noch keiner Prüfungsbehörde vorgelegen.

Darmstadt, den 23.3.2017

(Dipl.-Phys. Falk von Seggern)

A Acknowledgements

First of all, I would like to thank Prof. Horst Hahn for giving me the opportunity to work in his group. He provided the necessary funding and facilities to finish my thesis. With his support, I could benefit from collaboration with other scientists. Especially the time discussing scintific topics with him was particularly beneficial for my development as a scientist.

Second I would like to thank Prof. Jasmin Aghassi for frequent discussions and support as well as for being second referee of my thesis.

Further I would like to thank the other members of the examination committee, Prof. Ralph Krupke and Prof. Wolfgang Ensinger.

I would like to thank my direct supervisors Dr. Subho Dasgupta Dr. Ben Breitung for their continuous help throughout my thesis. They guided my research and always had an open mind for suggestions and scientific questions.

Dr. Robert Kruk as the brain of our group supported and helped me in countless discussions about scientific topics to understand their physical and chemical background.

I would like to thank Dr. Tessy Baby, who was my direct co-worker during the realization of the v-FET, which would not be realized without her help.

I am thankful to Dr. Anna Stösser who helped me in the laboratory especially with all chemical problems, which are not my speciallity.

I would like to express my gratitude to my fellow Ph.D. students Babak Nasr, Suresh Garlapati, Felix Neuper and Gabriel Marques who always had an ear and a helping hand to solve problems in and outside the laboratories of INT.

I would like to thank Ramona Hahn and Inna Schulz for their enormous support in the laboratories.

Special thanks go to Martin Limbach and Andreas Neumann, who helped me with the designing and building of the experimental equipments, maintained the sputtering system etc..

A very special thank is in order for Simone Dehm, who taught me SEM and E-beam lithography. Without her the preparation of samples would have been much slower.

My special thanks go to the entire “Tunable Group”, in particular to Dr. Philipp Leufke, Dr. Christian Reitz ,Dr. Ralf Witte, Dr. Arne Fischer, Dr. Thomas Reisinger and Alan Molinari. Many machines and devices designed, set up and maintained by all of them were mandatory for my experiments.

I want to thank the administrative staff of INT and TU-Darmstadt, Ms. Birgit Limmer, Ms. Renate Hernichel, Ms. Christine Fischer, Ms. Patricia Jaeger, for helping me with all kinds of paperwork at KIT and at TU Darmstadt.

I am grateful for the support of the “TEM Group”, in particular to Dr. Christian Kübel, Dr. Di Wang, Dr. Kiran Chakravadhanula and Torsten Scherer, for performing sample preparation using FIB and measurements at the TEM.

Torsten Scherer is also to be thanked for his tireless work for making the INT a more social and friendly place.

I would like to thank our collaborators Prof. Wolfgang Wenzel, Dr. Pascal Friedrich and Manuel Rommel for the simulation calculations and many discussions.

I am thankful for the financial support by the Deutsche Forschungsgemeinschaft (DFG), the Helmholtz Gemeinschaft in the form of Helmholtz Virtual Institute VI530, the Programme Science and Technology of Nanosystems (STN) and the Center for Functional Nanostructures (CFN) at KIT.

I would like to thank all my friends for their support during my thesis. The list on names would be too long.

A big thank you goes to my parents Heinz and Traute as well as my sister and her familiy for investing so much time and giving support in hard times especially during the final months of my thesis.

Last but not the least, I would like thank my wife Jördis who gave me the biggest gift in the world our son Emil. Also she beared my moods when I came home late and was stressed out and gave me a warm and beautiful place to come home to.

Without all of you this would not have been possible. THANKS!!!

B Personal data

B.1 Curriculum vitae (Lebenslauf)

Persönliche Daten

Name:	Falk von Seggern
Geburtsdatum:	24.03.1983
Geburtsort:	Summit, New Jersey (USA)
Staatsangehörigkeit:	deutsch/USA
Familienstand:	verheiratet; ein Sohn

Studium

Jan. 2017 – Apr. 2017	Promotionsstudent an der TUD, Fachbereich Material- und Geowissenschaften
Okt. 2003 – Jan. 2010	Studium der Physik, Ruprecht-Karl-Universität Heidelberg, Diplomarbeit am Kirchhoff Institut für Physik (KIP): Development of a metallic magnetic calorimeter for a neutrino mass measurement based on the EC-decay spectrum of ^{163}Ho

Schulbildung

Jun. 2002	Altes Kurfürstliches Gymnasium Bensheim, Allgemeine Hochschulreife

Berufstätigkeit

Jan. 2016 – Apr. 2017	Wissenschaftlicher Mitarbeiter im Gemeinschaftslabor Nanomaterialien TUD/KIT am INT
Apr. 2015 – Dez. 2015	Wissenschaftlicher Mitarbeiter am INT/KIT
Feb. 2011 – Apr. 2015	Wissenschaftlicher Mitarbeiter im Gemeinschaftslabor Nanomaterialien TUD/KIT am INT
Jan. 2008 – Jan. 2011	Werksstudent/Angestellter im Bereich Produktion und Qualitätsmanagement, SD-H, Heidelberg

Elternzeit

21. Sep. 2016 – 20. Nov. 2016	1. Elternzeit
21. Jan. 2017 – 20. Feb. 2017	2. Elternzeit

B.2 Publication List

- **von Seggern, F.**; Keskin, I.; Koos, E.; Kruk, R.; Hahn, H.; Dasgupta, S. Temperature-Dependent Performance of Printed Field-Effect Transistors with Solid Polymer Electrolyte Gating. ACS Appl. Mater. Interfaces 2016, 8 (46), 31757–31763.
- Baby, T. T.; Rommel, M.; **von Seggern, F.**; Friederich, P.; Reitz, C.; Dehm, S.; Kübel, C.; Wenzel, W.; Hahn, H.; Dasgupta, S. Sub-50 Nm Channel Vertical Field-Effect Transistors Using Conventional Ink-Jet Printing. Adv. Mater. 2017, 29 (4), 1603858.
- Stoesser, A.; **von Seggern, F.**; Purohit, S.; Nasr, B.; Kruk, R.; Dehm, S.; Di Wang; Hahn, H.; Dasgupta, S. Facile Fabrication of Electrolyte-Gated Single-Crystalline Cuprous Oxide Nanowire Field-Effect Transistors. Nanotechnology 2016, 27 (41), 415205.
- Sedlmaier, S. J.; Indris, S.; Dietrich, C.; Yavuz, M.; Dräger, C.; **von Seggern, F.**; Sommer, H.; Janek, J. Li 4 PS 4 I: A Li + Superionic Conductor Synthesized by a Solvent-Based Soft Chemistry Approach. Chem. Mater. 2017, 29 (4), 1830–1835.

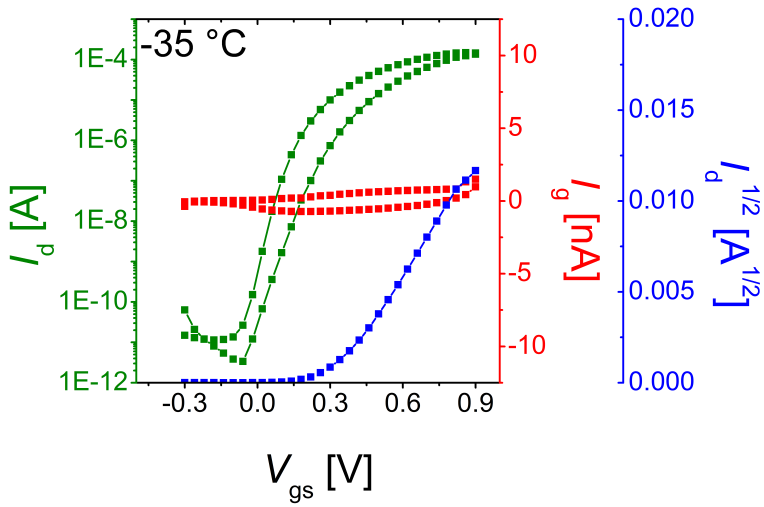
List of Figures

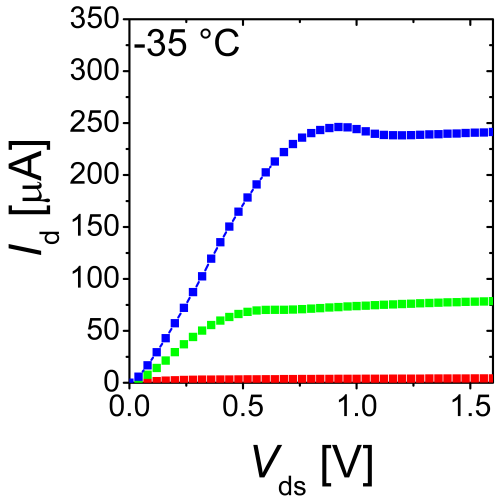
List of Tables

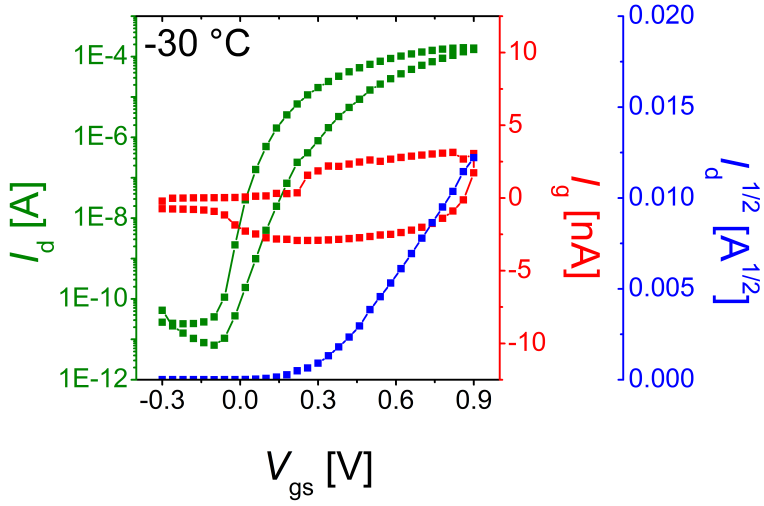
CSPE	composite solid polymer electrolyte
CSPE(lq)	as prepared composite solid polymer electrolyte before solidification
CSPE(sd)	composite solid polymer electrolyte after solidification
FET	field-effect transistors
EG-FET	electrolyte gated field-effect transistor
v-FET	vertical FET
DSC	differential scanning calorimetry
DOD	drop on demand
SC	semiconductor
LED	light emitting diode
ITO	tin doped indium oxide
MOSFET	metal oxide semiconductor FET
KLE	poly(ethylene-co-buthylene)-block-poly(ethylene oxide)
PEO	polyethylene oxide
PVA	polyvinyl alcohol
PIB-*b*-PEO	poly(isobuthylene)-block-poly(ethylene oxide)
DMSO	dimethyl sulfoxide
IR	infrared
PMMA	poly(methyl methacrylate)
SEM	scanning electron microscopy
TEM	transmission electron microscopy
SAED	selected area electron diffraction
STEM	scanning TEM
GIXRD	grazing incidence X-ray diffraction
PC	propylene carbonate
DEC	diethyl carbonate
EMC	ethyl methyl carbonate
DMC	dimethyl carbonate
CPE	constant phase element
RC-circuit	resistor and capacitor connected in parallel
VTF model	Vogel Tamman Fulcher model
I_{d}	drain-current
μ_{FET}	field effect mobility
SS	subthreshold slope
V_{th}	threshold voltage

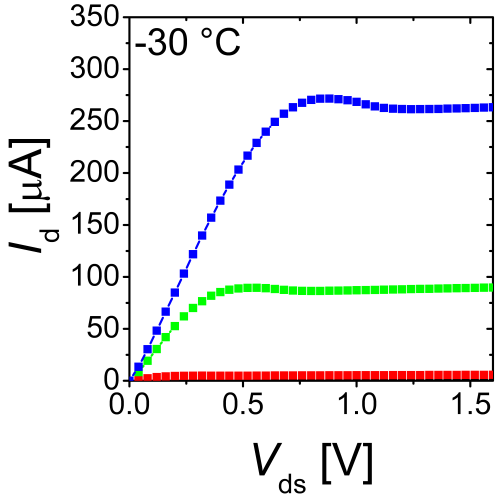
f_{co}	cut-off frequency
L	channel length
W	channel width
V_{ds}	drain-source current
V_{gs}	gate-voltage
a	slope of the ${I_{\mathrm{d}}}^{1/2}$ curve in the linear regime
$\lvert Z \rvert$	absolute impedance
Z'	real part of $\lvert Z \rvert$
Z''	imaginary part of $\lvert Z \rvert$
ω	radial frequency
φ	phase angle
C'	capacitance
C	areal capacitance
R_{ext}	resistance of all leads between PPC and EIS
C'_{ext}	capacitance of all leads between PPC and EIS
C_{dl}	areal double layer capacitance
C'_{dl}	double layer capacitance
R_{el}	electrolyte resistance
σ_{el}	electrolyte conductivity
R_{hyd}	hydrodynamic radius
T	absolute temperature
η	semiconductor to bulk volume ratio

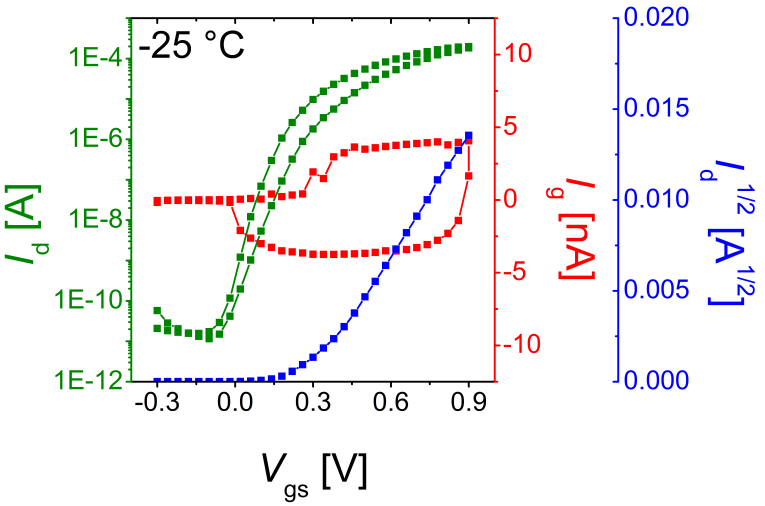
C Transfer and Output Curves of all Temperatures for In-Plane FET

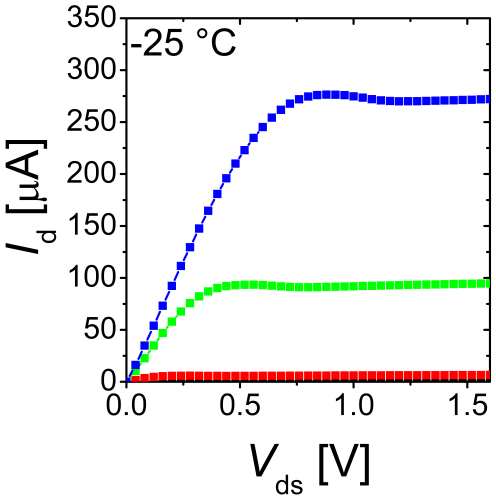


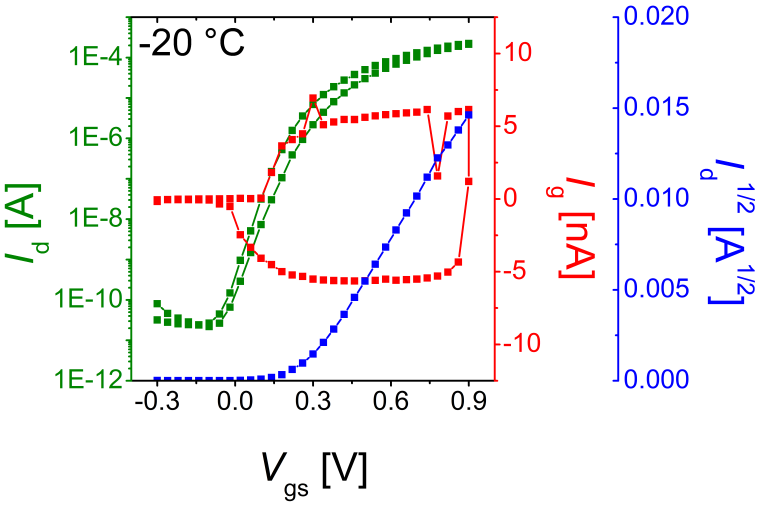


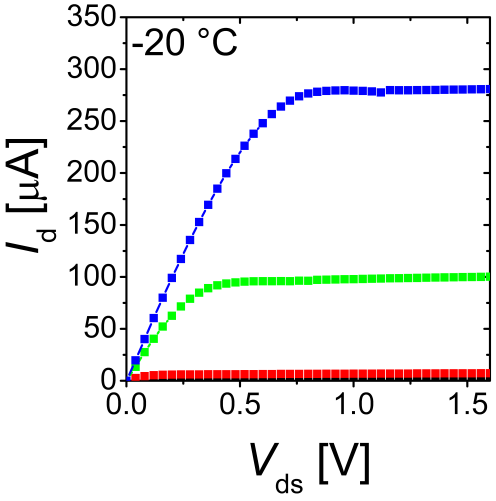


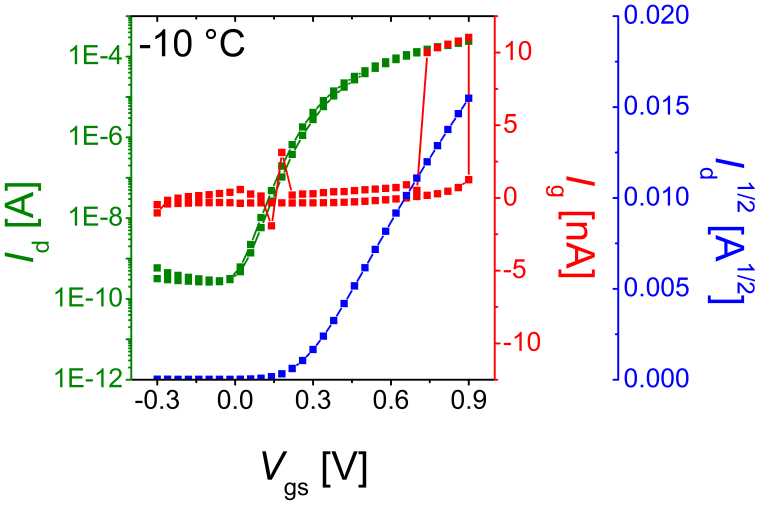


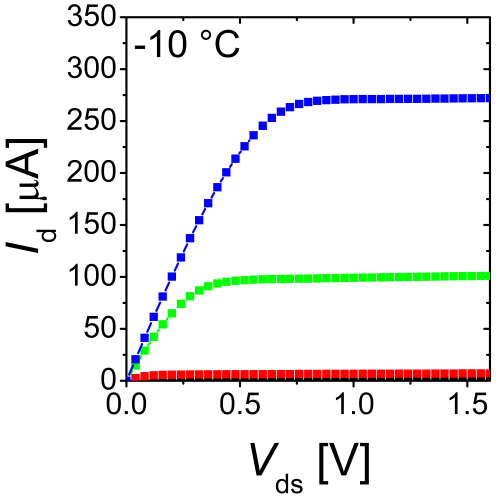

-25 °C
1E-4
1E-6
1E-8
1E-10
1E-12
I_d [A]
10
5
0
-5
-10
I_g [nA]
0.020
0.015
0.010
0.005
0.000
$I_d^{1/2}$ [$A^{1/2}$]
-0.3
0.0
0.3
0.6
0.9
V_{gs} [V]

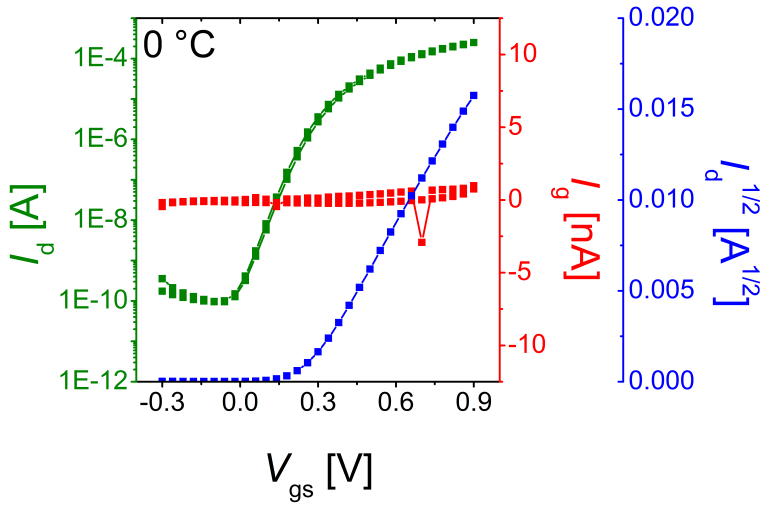

-25 °C
350
300
250
200
150
100
50
0
I_d [µA]
0.0
0.5
1.0
1.5
V_{ds} [V]

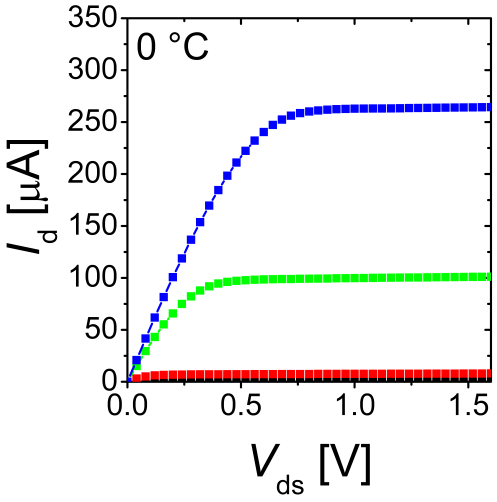

-20 °C
1E-4
1E-6
1E-8
1E-10
1E-12
I_d [A]
10
5
0
-5
-10
I_g [nA]
0.020
0.015
0.010
0.005
0.000
$I_d^{1/2}$ [$A^{1/2}$]
-0.3
0.0
0.3
0.6
0.9
V_{gs} [V]

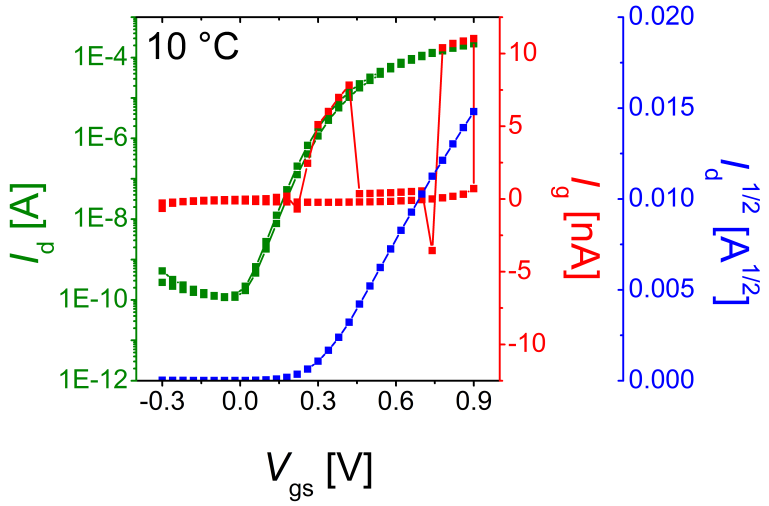

-20 °C
350
300
250
200
150
100
50
0
I_d [µA]
0.0
0.5
1.0
1.5
V_{ds} [V]

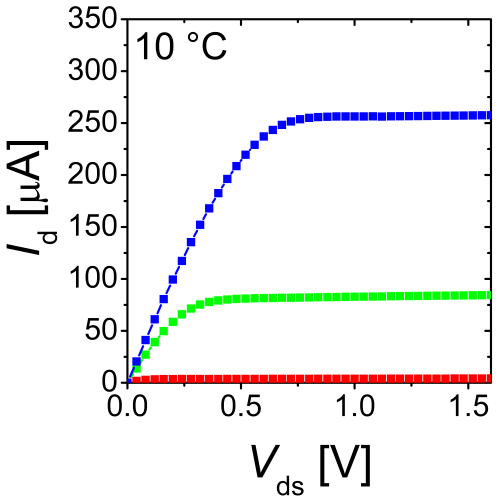

-10 °C
1E-4
1E-6
1E-8
1E-10
1E-12
I_d [A]
10
5
0
-5
-10
I_g [nA]
0.020
0.015
0.010
0.005
0.000
$I_d^{1/2}$ [$A^{1/2}$]
-0.3
0.0
0.3
0.6
0.9
V_{gs} [V]

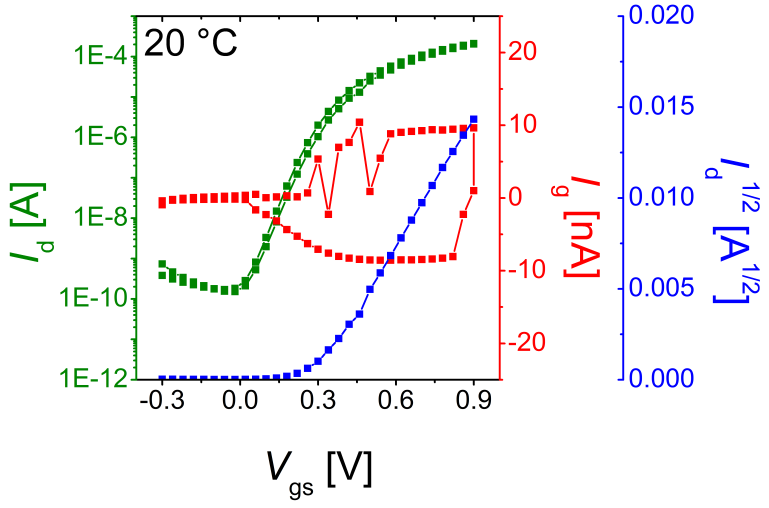

-10 °C
350
300
250
200
150
100
50
0
I_d [µA]
0.0
0.5
1.0
1.5
V_{ds} [V]

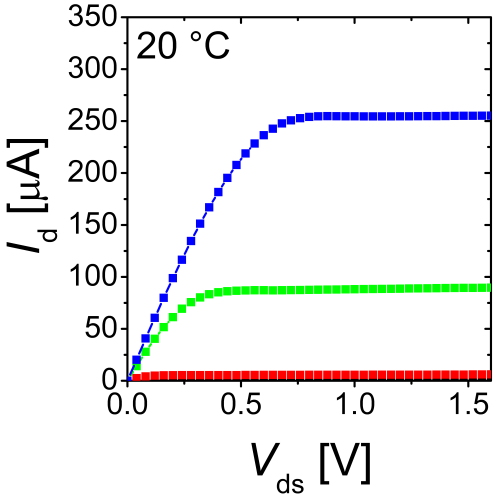

0 °C
1E-4
1E-6
1E-8
1E-10
1E-12
I_d [A]
10
5
0
-5
-10
I_g [nA]
0.020
0.015
0.010
0.005
0.000
$I_d^{1/2}$ [$A^{1/2}$]
-0.3
0.0
0.3
0.6
0.9
V_{gs} [V]

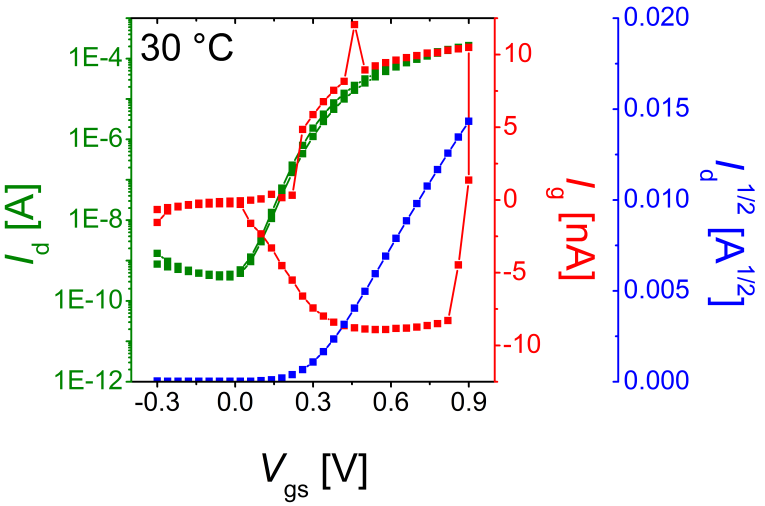

0 °C
350
300
250
200
150
100
50
0
I_d [µA]
0.0
0.5
1.0
1.5
V_{ds} [V]

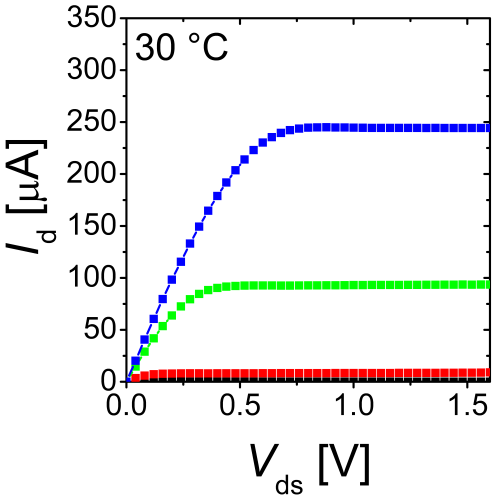

10 °C
1E-4
1E-6
1E-8
1E-10
1E-12
I_d [A]
10
5
0
-5
-10
I_g [nA]
0.020
0.015
0.010
0.005
0.000
$I_d^{1/2}$ [$A^{1/2}$]
-0.3
0.0
0.3
0.6
0.9
V_{gs} [V]

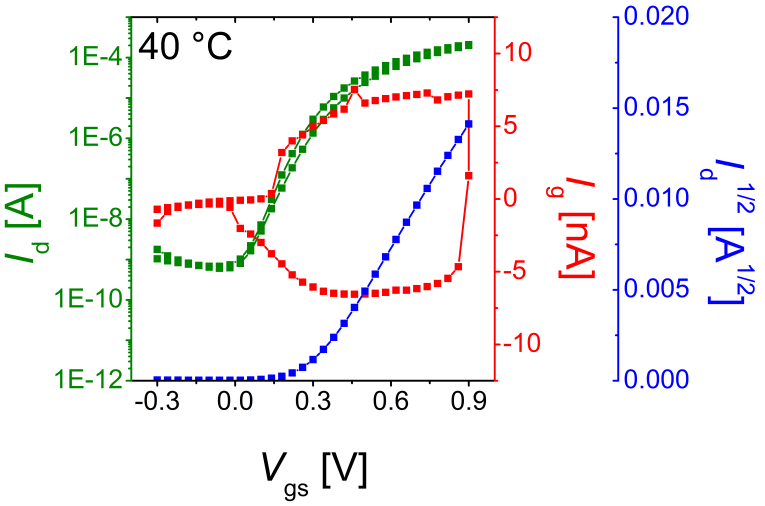

10 °C
350
300
250
200
150
100
50
0
I_d [µA]
0.0
0.5
1.0
1.5
V_{ds} [V]

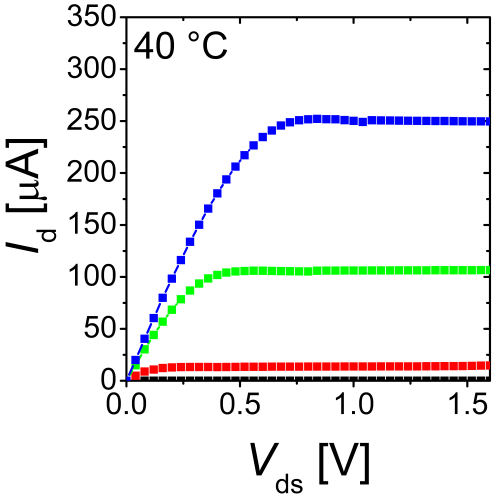

20 °C
1E-4
1E-6
1E-8
1E-10
1E-12
I_d [A]
20
10
0
-10
-20
I_g [nA]
0.020
0.015
0.010
0.005
0.000
$I_d^{1/2}$ [$A^{1/2}$]
-0.3
0.0
0.3
0.6
0.9
V_{gs} [V]

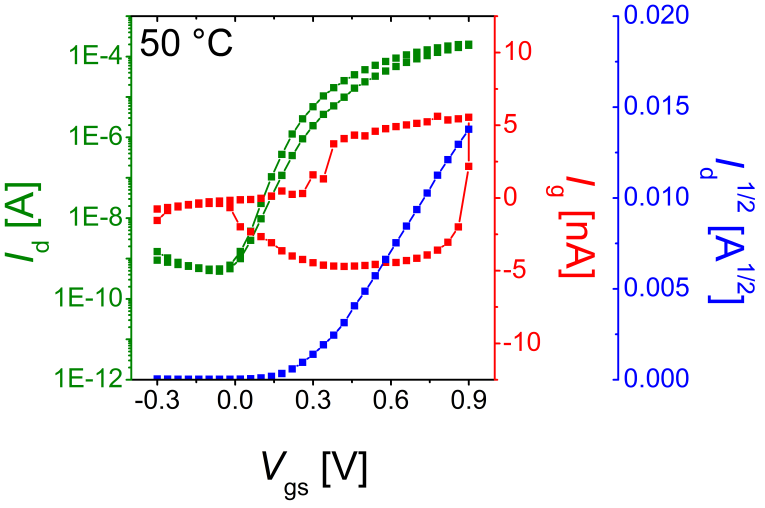

20 °C
350
300
250
200
150
100
50
0
I_d [µA]
0.0
0.5
1.0
1.5
V_{ds} [V]

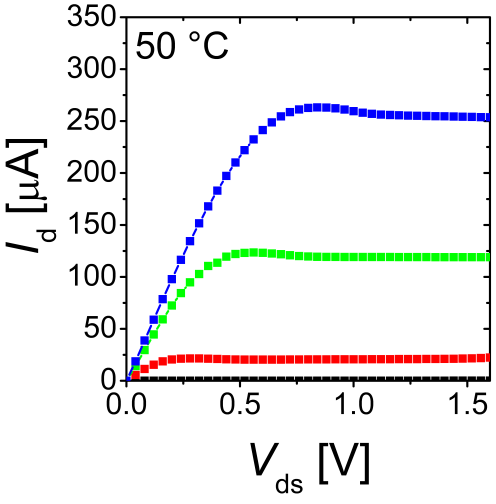

30 °C
1E-4
1E-6
1E-8
1E-10
1E-12
I_d [A]
10
5
0
-5
-10
I_g [nA]
0.020
0.015
0.010
0.005
0.000
$I_d^{1/2}$ [$A^{1/2}$]
-0.3
0.0
0.3
0.6
0.9
V_{gs} [V]

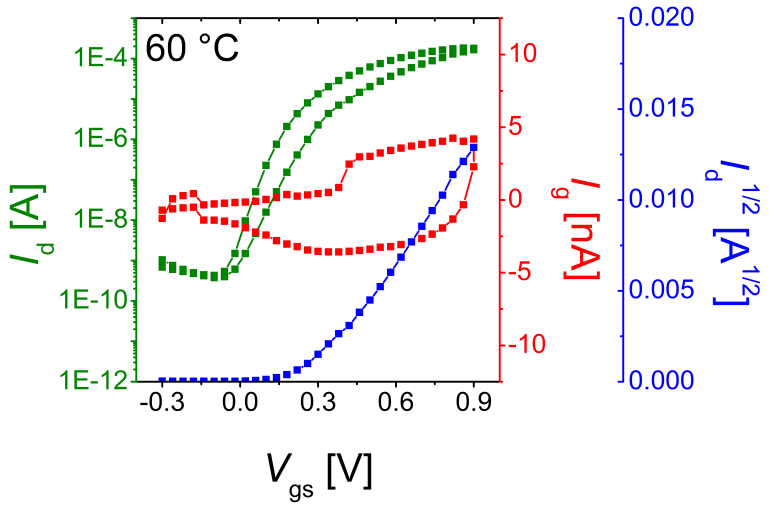

30 °C
350
300
250
200
150
100
50
0
I_d [µA]
0.0
0.5
1.0
1.5
V_{ds} [V]

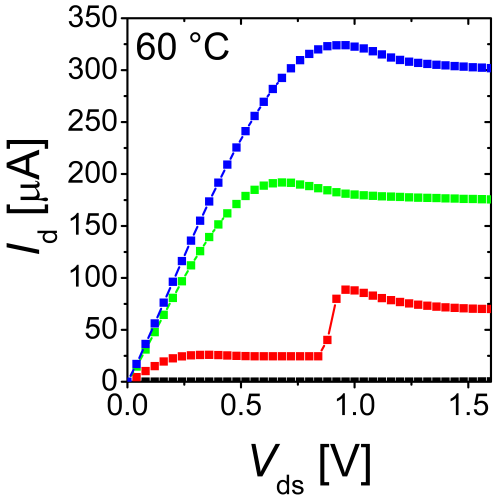

40 °C
1E-4
1E-6
1E-8
1E-10
1E-12
I_d [A]
10
5
0
-5
-10
I_g [nA]
0.020
0.015
0.010
0.005
0.000
$I_d^{1/2}$ [$A^{1/2}$]
-0.3
0.0
0.3
0.6
0.9
V_{gs} [V]

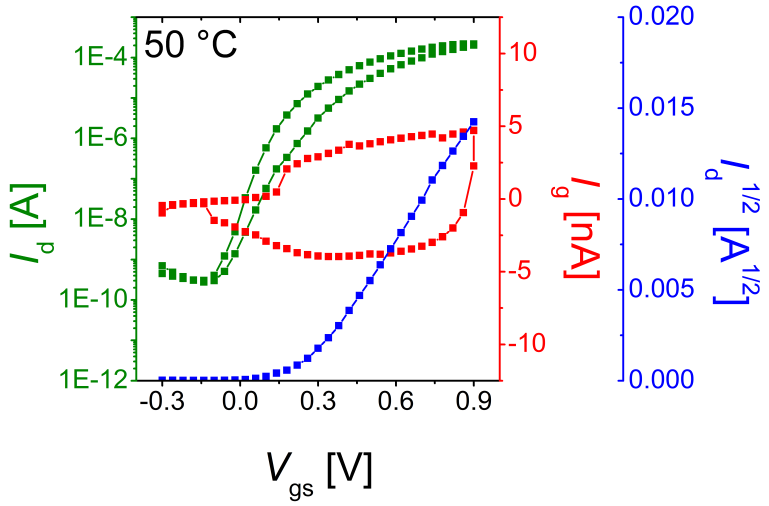

40 °C
350
300
250
200
150
100
50
0
I_d [µA]
0.0
0.5
1.0
1.5
V_{ds} [V]

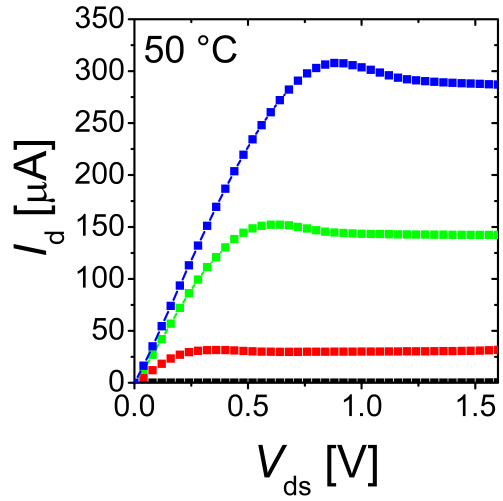

50 °C
1E-4
1E-6
1E-8
1E-10
1E-12
I_d [A]
10
5
0
-5
-10
I_g [nA]
0.020
0.015
0.010
0.005
0.000
$I_d^{1/2}$ [$A^{1/2}$]
-0.3
0.0
0.3
0.6
0.9
V_{gs} [V]

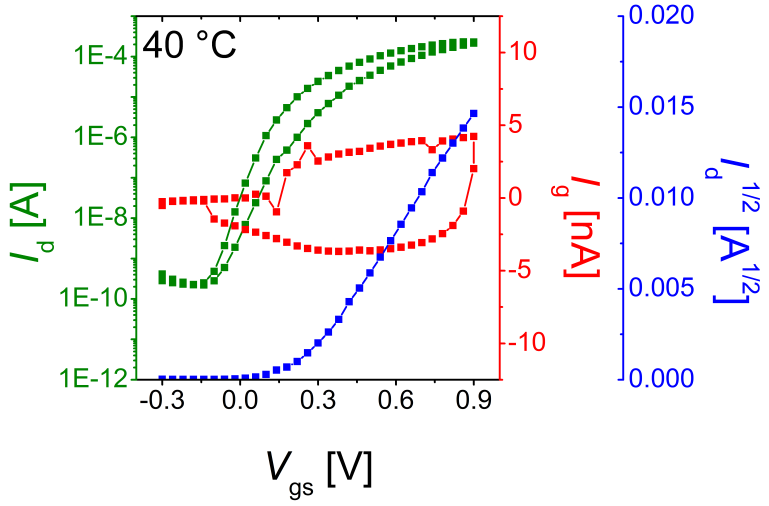

50 °C
350
300
250
200
150
100
50
0
I_d [µA]
0.0
0.5
1.0
1.5
V_{ds} [V]

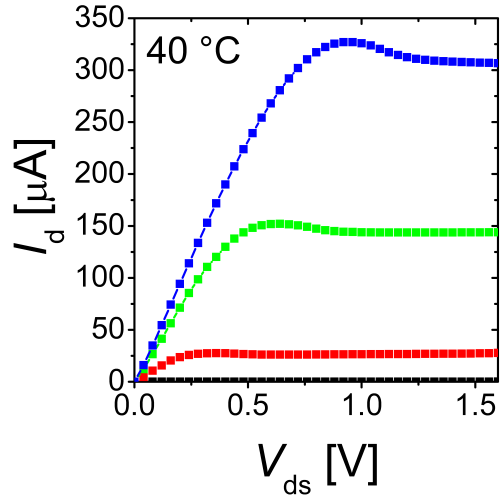

60 °C
1E-4
1E-6
1E-8
1E-10
1E-12
I_d [A]
10
5
0
-5
-10
I_g [nA]
0.020
0.015
0.010
0.005
0.000
$I_d^{1/2}$ [$A^{1/2}$]
-0.3
0.0
0.3
0.6
0.9
V_{gs} [V]

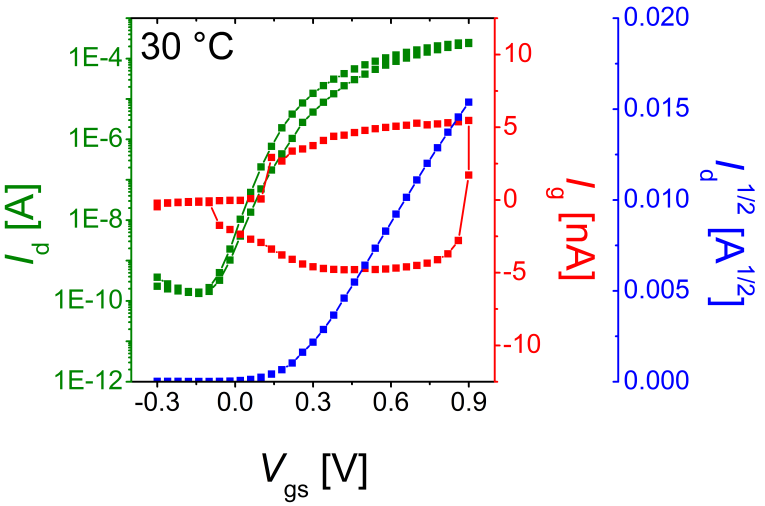

60 °C
350
300
250
200
150
100
50
0
I_d [µA]
0.0
0.5
1.0
1.5
V_{ds} [V]

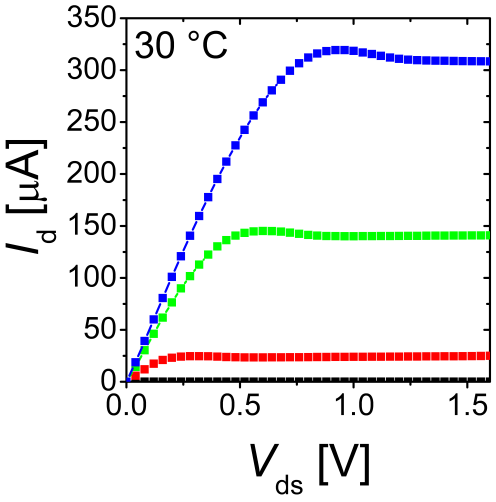

50 °C
1E-4
1E-6
1E-8
1E-10
1E-12
I_d [A]
10
5
0
-5
-10
I_g [nA]
0.020
0.015
0.010
0.005
0.000
$I_d^{1/2}$ [$A^{1/2}$]
-0.3
0.0
0.3
0.6
0.9
V_{gs} [V]

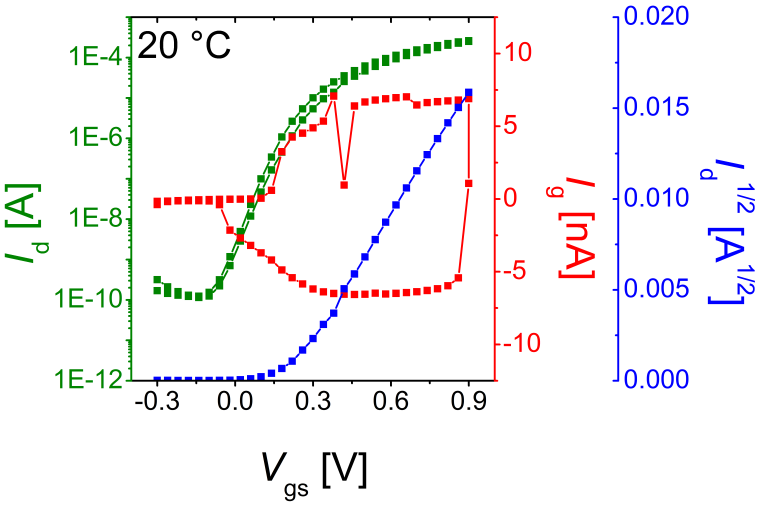

50 °C
350
300
250
200
150
100
50
0
I_d [µA]
0.0
0.5
1.0
1.5
V_{ds} [V]

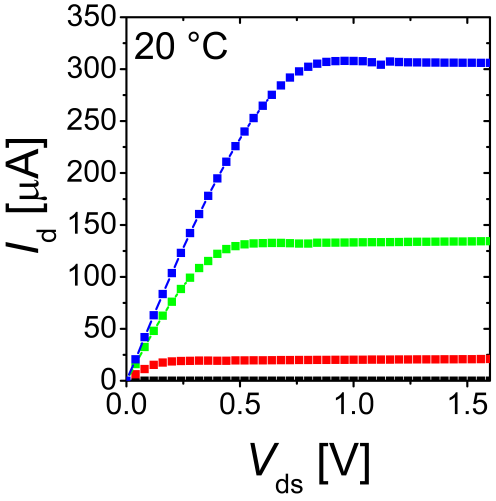

40 °C
1E-4
1E-6
1E-8
1E-10
1E-12
I_d [A]
10
5
0
-5
-10
I_g [nA]
0.020
0.015
0.010
0.005
0.000
$I_d^{1/2}$ [$A^{1/2}$]
-0.3
0.0
0.3
0.6
0.9
V_{gs} [V]

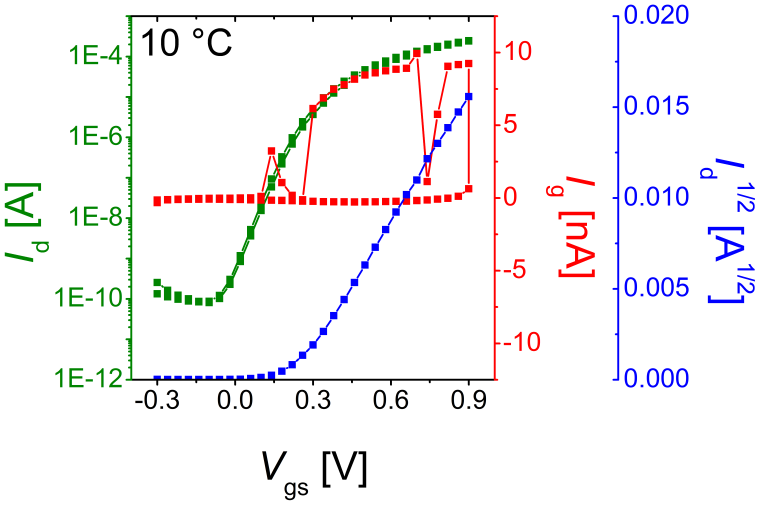

40 °C
350
300
250
200
150
100
50
0
I_d [µA]
0.0
0.5
1.0
1.5
V_{ds} [V]

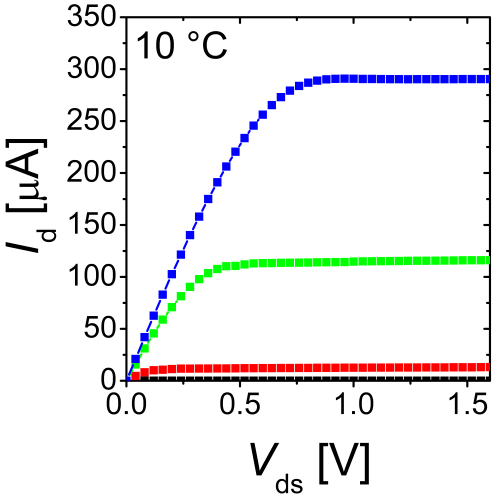

30 °C
1E-4
1E-6
1E-8
1E-10
1E-12
I_d [A]
10
5
0
-5
-10
I_g [nA]
0.020
0.015
0.010
0.005
0.000
$I_d^{1/2}$ [$A^{1/2}$]
-0.3
0.0
0.3
0.6
0.9
V_{gs} [V]

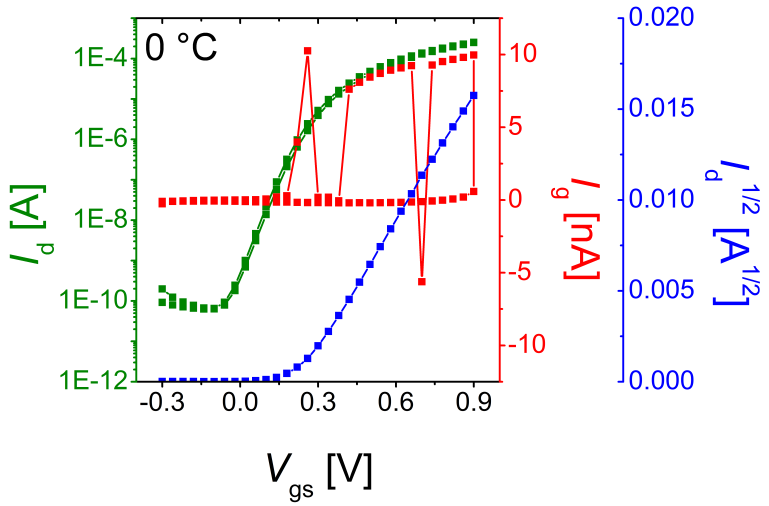

30 °C
350
300
250
200
150
100
50
0
I_d [µA]
0.0
0.5
1.0
1.5
V_{ds} [V]

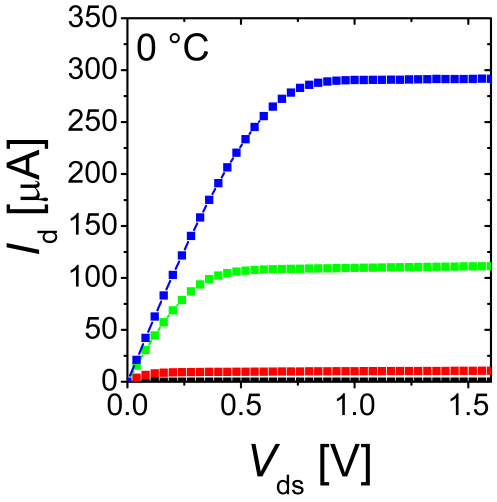

20 °C
1E-4
1E-6
1E-8
1E-10
1E-12
I_d [A]
10
5
0
-5
-10
I_g [nA]
0.020
0.015
0.010
0.005
0.000
$I_d^{1/2}$ [$A^{1/2}$]
-0.3
0.0
0.3
0.6
0.9
V_{gs} [V]

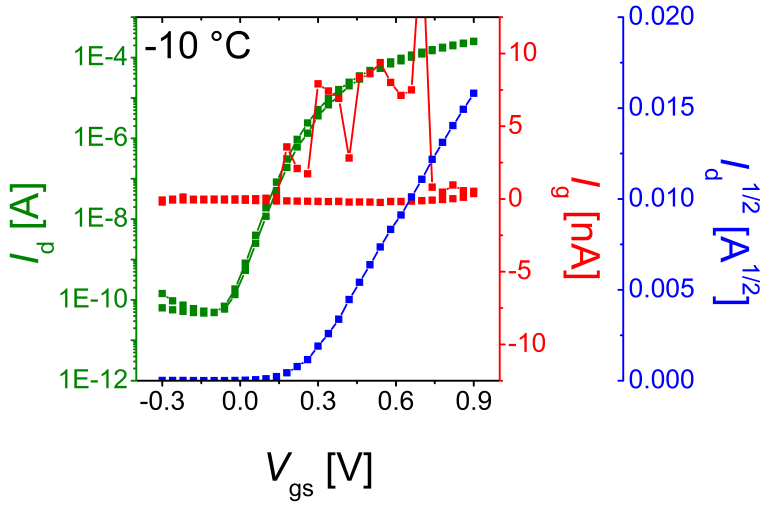

20 °C
350
300
250
200
150
100
50
0
I_d [µA]
0.0
0.5
1.0
1.5
V_{ds} [V]

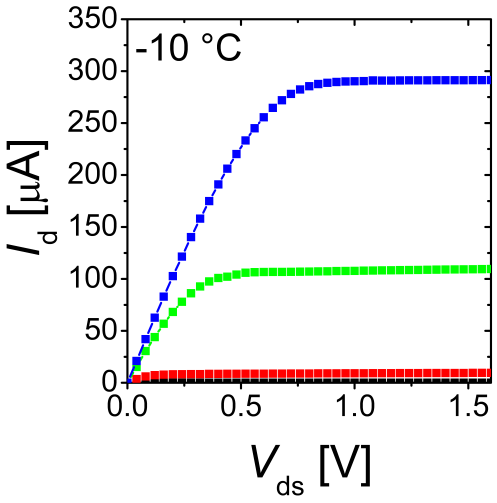

10 °C
1E-4
1E-6
1E-8
1E-10
1E-12
I_d [A]
10
5
0
-5
-10
I_g [nA]
0.020
0.015
0.010
0.005
0.000
$I_d^{1/2}$ [$A^{1/2}$]
-0.3
0.0
0.3
0.6
0.9
V_{gs} [V]

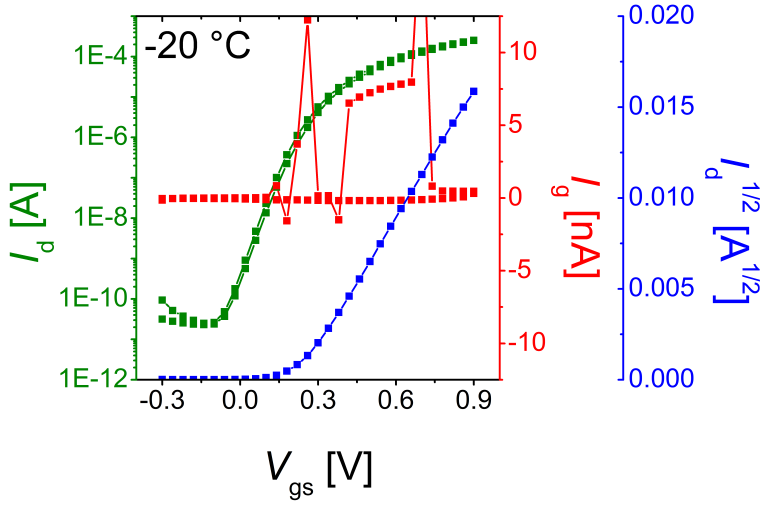

10 °C
350
300
250
200
150
100
50
0
I_d [µA]
0.0
0.5
1.0
1.5
V_{ds} [V]

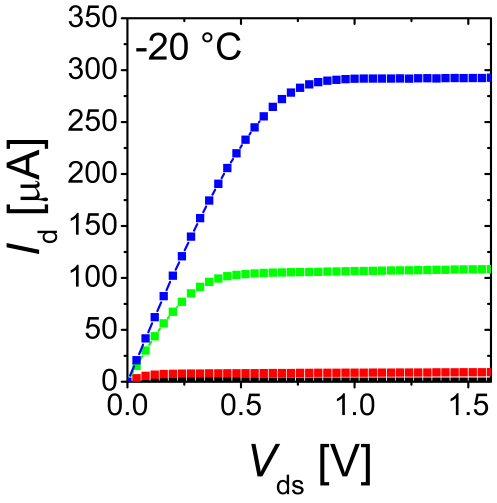

0 °C
1E-4
1E-6
1E-8
1E-10
1E-12
I_d [A]
10
5
0
-5
-10
I_g [nA]
0.020
0.015
0.010
0.005
0.000
$I_d^{1/2}$ [$A^{1/2}$]
-0.3
0.0
0.3
0.6
0.9
V_{gs} [V]


0 °C
350
300
250
200
150
100
50
0
I_d [µA]
0.0
0.5
1.0
1.5
V_{ds} [V]


-10 °C
1E-4
1E-6
1E-8
1E-10
1E-12
I_d [A]
10
5
0
-5
-10
I_g [nA]
0.020
0.015
0.010
0.005
0.000
$I_d^{1/2}$ [$A^{1/2}$]
-0.3
0.0
0.3
0.6
0.9
V_{gs} [V]


-10 °C
350
300
250
200
150
100
50
0
I_d [µA]
0.0
0.5
1.0
1.5
V_{ds} [V]


-20 °C
1E-4
1E-6
1E-8
1E-10
1E-12
I_d [A]
10
5
0
-5
-10
I_g [nA]
0.020
0.015
0.010
0.005
0.000
$I_d^{1/2}$ [$A^{1/2}$]
-0.3
0.0
0.3
0.6
0.9
V_{gs} [V]


-20 °C
350
300
250
200
150
100
50
0
I_d [µA]
0.0
0.5
1.0
1.5
V_{ds} [V]

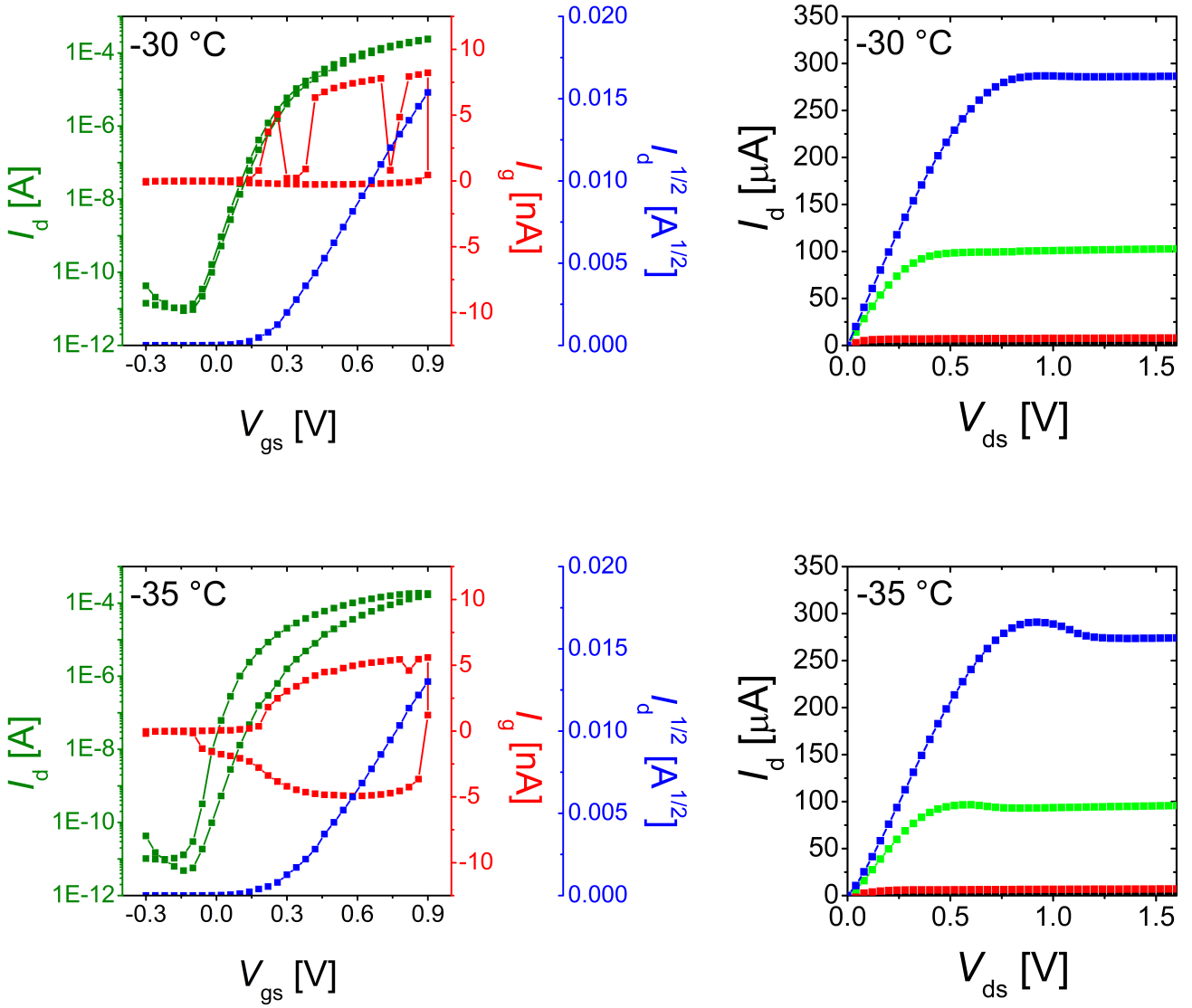


Figure C.1.: On the left hand side the transfer curve (green) measued at V_{ds}=1 V, the leakage current (red) and the $I_d{}^{1/2}$ curve is plotted vs. V_{gs}. On the right hand side the corresponding output curves (V_{gs}=0.0 V (black), V_{gs}=0.3 V (red), V_{gs}=0.6 V (green) and V_{gs}=0.9 V (blue) are plotted vs. V_{ds}. The respective temperature is written in the upper left corner of the graph.

D Full Set of Impedance Data Fitted with the EC from Figure 4.4(b)

Table D.1.: List of all measured impedance data of CSPE-1 for different temperatures with a fixed external resistance of 4 kΩ.

Temperature [°C]	R_{el} [Ω]	Warburg R [Ω]	Warburg C [F]	Warburg α a.u.	C_{dl} [F]	$\alpha(C_{dl})$ a.u.	C'_{ext} [F]
46	207,9	1035	$1{,}34{\cdot}10^{-4}$	0,5	$1{,}35{\cdot}10^{-7}$	0,95	$1{,}85{\cdot}10^{-10}$
33	357,3	890,1	$1{,}38{\cdot}10^{-4}$	0,5	$1{,}31{\cdot}10^{-7}$	0,95	$1{,}84{\cdot}10^{-10}$
22	548,7	881,2	$1{,}71{\cdot}10^{-4}$	0,5	$1{,}19{\cdot}10^{-7}$	0,96	$1{,}83{\cdot}10^{-10}$
10	755,9	853,3	$2{,}02{\cdot}10^{-4}$	0,5	$1{,}12{\cdot}10^{-7}$	0,96	$1{,}82{\cdot}10^{-10}$
-1	1004	847	$2{,}33{\cdot}10^{-4}$	0,5	$1{,}08{\cdot}10^{-7}$	0,96	$1{,}82{\cdot}10^{-10}$
-12	1346	1008	$3{,}07{\cdot}10^{-4}$	0,5	$1{,}02{\cdot}10^{-7}$	0,97	$1{,}81{\cdot}10^{-10}$
-23	1818	1287	$3{,}74{\cdot}10^{-4}$	0,5	$9{,}82{\cdot}10^{-8}$	0,96	$1{,}81{\cdot}10^{-10}$
-33	3001	4246	$7{,}45{\cdot}10^{-4}$	0,5	$1{,}01{\cdot}10^{-7}$	0,96	$1{,}79{\cdot}10^{-10}$
-44	5220	12963	$1{,}68{\cdot}10^{-3}$	0,5	$9{,}41{\cdot}10^{-8}$	0,96	$1{,}76{\cdot}10^{-10}$
-34	3512	6516	$9{,}89{\cdot}10^{-4}$	0,5	$9{,}61{\cdot}10^{-8}$	0,96	$1{,}78{\cdot}10^{-10}$
-23	2094	2637	$5{,}24{\cdot}10^{-4}$	0,5	$1{,}00{\cdot}10^{-7}$	0,96	$1{,}8{\cdot}10^{-10}$
-12	1332	904,7	$2{,}84{\cdot}10^{-4}$	0,5	$1{,}06{\cdot}10^{-7}$	0,96	$1{,}82{\cdot}10^{-10}$
-1	1006	875,2	$2{,}51{\cdot}10^{-4}$	0,5	$1{,}05{\cdot}10^{-7}$	0,96	$1{,}82{\cdot}10^{-10}$
10	753	852,5	$2{,}10{\cdot}10^{-4}$	0,5	$1{,}11{\cdot}10^{-7}$	0,96	$1{,}83{\cdot}10^{-10}$
22	559,4	880,4	$1{,}79{\cdot}10^{-4}$	0,5	$1{,}18{\cdot}10^{-7}$	0,96	$1{,}83{\cdot}10^{-10}$
34	369,2	958	$1{,}54{\cdot}10^{-4}$	0,5	$1{,}26{\cdot}10^{-7}$	0,96	$1{,}84{\cdot}10^{-10}$
46	224,1	1024	$1{,}40{\cdot}10^{-4}$	0,5	$1{,}39{\cdot}10^{-7}$	0,95	$1{,}83{\cdot}10^{-10}$

Table D.2.: List of all measured impedance data of CSPE-2 for different temperatures with a fixed external resistance of 4 kΩ.

Temperature [°C]	R_{el} [Ω]	Warburg R [Ω]	Warburg C [F]	Warburg α a.u.	C_{dl} [F]	$\alpha(C_{dl})$ a.u.	C'_{ext} [F]
46	1022	385,6	$1{,}17{\cdot}10^{-4}$	0,5	$1{,}27{\cdot}10^{-7}$	0,95	$1{,}74{\cdot}10^{-10}$
33	1217	344,3	$1{,}47{\cdot}10^{-4}$	0,5	$1{,}17{\cdot}10^{-7}$	0,95	$1{,}75{\cdot}10^{-10}$
22	1471	399,4	$2{,}18{\cdot}10^{-4}$	0,5	$1{,}07{\cdot}10^{-7}$	0,96	$1{,}74{\cdot}10^{-10}$
10	1826	361,2	$2{,}40{\cdot}10^{-4}$	0,5	$1{,}03{\cdot}10^{-7}$	0,96	$1{,}74{\cdot}10^{-10}$
-1	2324	451,1	$3{,}05{\cdot}10^{-4}$	0,5	$1{,}00{\cdot}10^{-7}$	0,96	$1{,}66{\cdot}10^{-10}$
-12	3153	843,7	$4{,}71{\cdot}10^{-4}$	0,5	$9{,}25{\cdot}10^{-8}$	0,97	$1{,}67{\cdot}10^{-10}$
-23	4688	1548	$6{,}69{\cdot}10^{-4}$	0,5	$8{,}98{\cdot}10^{-8}$	0,97	$1{,}69{\cdot}10^{-10}$
-33	7704	3748	$1{,}15{\cdot}10^{-3}$	0,5	$8{,}43{\cdot}10^{-8}$	0,97	$1{,}69{\cdot}10^{-10}$
-44	14770	10651	$2{,}13{\cdot}10^{-3}$	0,5	$8{,}24{\cdot}10^{-8}$	0,97	$1{,}68{\cdot}10^{-10}$
-34	7917	3426	$1{,}09{\cdot}10^{-3}$	0,5	$8{,}61{\cdot}10^{-8}$	0,97	$1{,}69{\cdot}10^{-10}$
-23	4778	1541	$7{,}00{\cdot}10^{-4}$	0,5	$9{,}02{\cdot}10^{-8}$	0,97	$1{,}7{\cdot}10^{-10}$
-12	3156	802,9	$4{,}84{\cdot}10^{-4}$	0,5	$9{,}30{\cdot}10^{-8}$	0,97	$1{,}71{\cdot}10^{-10}$
-1	2429	503,6	$3{,}41{\cdot}10^{-4}$	0,5	$9{,}76{\cdot}10^{-8}$	0,96	$1{,}72{\cdot}10^{-10}$
10	1843	375,9	$2{,}59{\cdot}10^{-4}$	0,5	$1{,}02{\cdot}10^{-7}$	0,96	$1{,}73{\cdot}10^{-10}$
22	1530	319,2	$2{,}00{\cdot}10^{-4}$	0,5	$1{,}08{\cdot}10^{-7}$	0,96	$1{,}74{\cdot}10^{-10}$
34	1226	362,4	$1{,}60{\cdot}10^{-4}$	0,5	$1{,}15{\cdot}10^{-7}$	0,96	$1{,}74{\cdot}10^{-10}$
46	1058	400,1	$1{,}32{\cdot}10^{-4}$	0,5	$1{,}25{\cdot}10^{-7}$	0,95	$1{,}75{\cdot}10^{-10}$

Table D.3.: List of all measured impedance data of CSP·10^{-3} for different temperatures with a fixed external resistance of 4 kΩ.

Temperature [°C]	R_{el} [Ω]	Warburg R [Ω]	Warburg C [F]	Warburg α a.u.	C_{dl} [F]	$\alpha(C_{dl})$ a.u.	C'_{ext} [F]
46	1240	585	$1{,}17{\cdot}10^{-4}$	0,5	$1{,}26{\cdot}10^{-7}$	0,95	$1{,}78{\cdot}10^{-10}$
33	1437	535,1	$1{,}46{\cdot}10^{-4}$	0,5	$1{,}17{\cdot}10^{-7}$	0,96	$1{,}76{\cdot}10^{-10}$
22	1692	526,6	$1{,}81{\cdot}10^{-4}$	0,5	$1{,}09{\cdot}10^{-7}$	0,96	$1{,}76{\cdot}10^{-10}$
10	2051	533,6	$2{,}26{\cdot}10^{-4}$	0,5	$1{,}06{\cdot}10^{-7}$	0,96	$1{,}75{\cdot}10^{-10}$
-1	2531	696,7	$2{,}96{\cdot}10^{-4}$	0,5	$1{,}01{\cdot}10^{-7}$	0,96	$1{,}75{\cdot}10^{-10}$
-12	3431	1137	$4{,}51{\cdot}10^{-4}$	0,5	$9{,}46{\cdot}10^{-8}$	0,97	$1{,}74{\cdot}10^{-10}$
-23	5149	1806	$5{,}88{\cdot}10^{-4}$	0,5	$9{,}39{\cdot}10^{-8}$	0,96	$1{,}71{\cdot}10^{-10}$
-33	8638	4847	$1{,}13{\cdot}10^{-3}$	0,5	$8{,}68{\cdot}10^{-8}$	0,97	$1{,}7{\cdot}10^{-10}$
-44	15997	14034	$2{,}30{\cdot}10^{-3}$	0,5	$8{,}36{\cdot}10^{-8}$	0,97	$1{,}7{\cdot}10^{-10}$
-34	8380	5067	$1{,}03{\cdot}10^{-3}$	0,5	$8{,}87{\cdot}10^{-8}$	0,96	$1{,}7{\cdot}10^{-10}$
-23	5210	2043	$6{,}51{\cdot}10^{-4}$	0,5	$9{,}26{\cdot}10^{-8}$	0,96	$1{,}72{\cdot}10^{-10}$
-12	3318	1035	$4{,}13{\cdot}10^{-4}$	0,5	$9{,}76{\cdot}10^{-8}$	0,96	$1{,}73{\cdot}10^{-10}$
-1	2467	653	$2{,}83{\cdot}10^{-4}$	0,5	$1{,}02{\cdot}10^{-7}$	0,96	$1{,}74{\cdot}10^{-10}$
10	1980	541,9	$2{,}26{\cdot}10^{-4}$	0,5	$1{,}05{\cdot}10^{-7}$	0,96	$1{,}75{\cdot}10^{-10}$
22	1670	447,8	$1{,}64{\cdot}10^{-4}$	0,5	$1{,}15{\cdot}10^{-7}$	0,95	$1{,}75{\cdot}10^{-10}$
34	1425	517,2	$1{,}43{\cdot}10^{-4}$	0,5	$1{,}19{\cdot}10^{-7}$	0,96	$1{,}76{\cdot}10^{-10}$
46	1236	568,3	$1{,}18{\cdot}10^{-4}$	0,5	$1{,}31{\cdot}10^{-7}$	0,95	$1{,}75{\cdot}10^{-10}$

E Solid Polymer Electrolytes

Table E.1.: List of solid polymer electrolytes with tensile strength and ionic conductivity values.

Solid polymer electrolytes	Conductivity [S cm^{-1}]	Tensile strength [MPa]	Temperature [°C]
BAB/LiClO4[84]	2×10^{-4}	15	30
PVA/SiO_2-g-HBPAE/$LiClO_4$[102]	1.5×10^{-4}	15	25
H_3PO_4/PVA[85]	3.4×10^{-3}	2	-
CSPE-1	8×10^{-3}	5.4	25

F Carbonates Suitable for Electrolyte Preparation

Table F.1.: Composition of as prepared CSPEs. The amounts are listed in gram.

solvent	viscosity (cP) (25 °C)	dielectric constant	melting point (°C)
PC	2.5	64.9	-48.8
DEC	0.75	2.8	-74.3
EMC	0.65	3.0	-53.0
EC	1.9 (40 °C)	89.8	36.4
DMC	0.59	3.1	4.6
DMSO	2	46.7	18

G Morphologies for Drift Diffusion Simulations

For the drift diffusion model simulation, three different morphologies of the porous semiconductor have been taken into account. One is the morphology of the as prepared semiconductor network extracted from a SEM micrograph, the other two are created using a Metropolis Monte-Carlo-based simulated annealing algorithm. With different times of simulation one system with smaller pore sizes and smaller ligament widths and one with larger pore sizes and filament widths are created. The three different morphologies are shown in Figure G.1

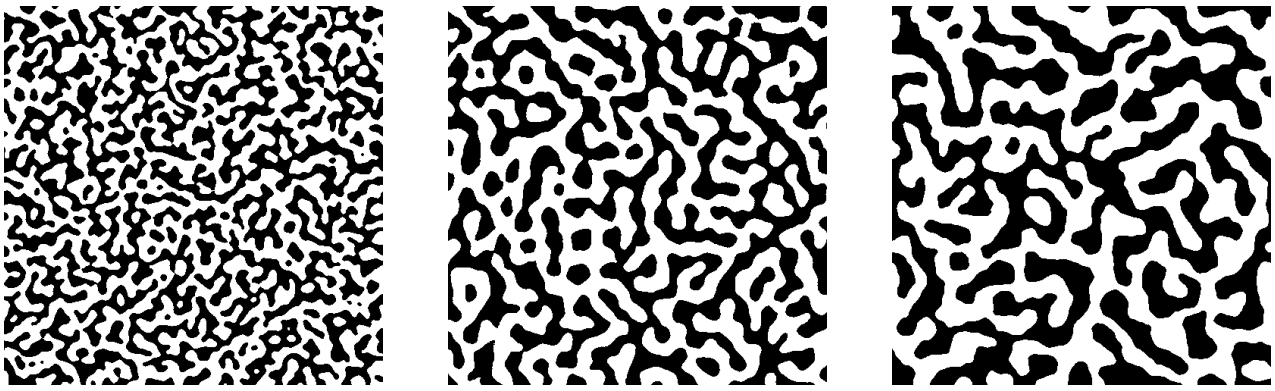


Figure G.1.: Pictures of three different semiconductor morphologies as used for the drift diffusion simulations. The morphologies in (a) and (c) are created by a Metropolis Monte-Carlo-based simulated annealing algorithm with differnt annealing times, picture (b) is a SEM micrograph of the as prepared porous SnO_2 network transfered into black and white.

H Calculation of Number of Pillars

For the horizontal channel back gate device from section 5.4 the number of pillars is calculated, using the geometrical specification from Figure 5.15 and results as follows:

$$V_{\text{bulk}} = W'_{\text{channel}} \cdot L \cdot d_{\text{channel}} = 50 \cdot 50 \cdot 0.05\,\mu m^3 \tag{H.1}$$

$$L = 50\,\mu m \tag{H.2}$$

$$R = 10\,nm \tag{H.3}$$

$$\eta = 51,7\,\% \tag{H.4}$$

$$\Rightarrow N_{\text{pillars}} = 4114 \tag{H.5}$$